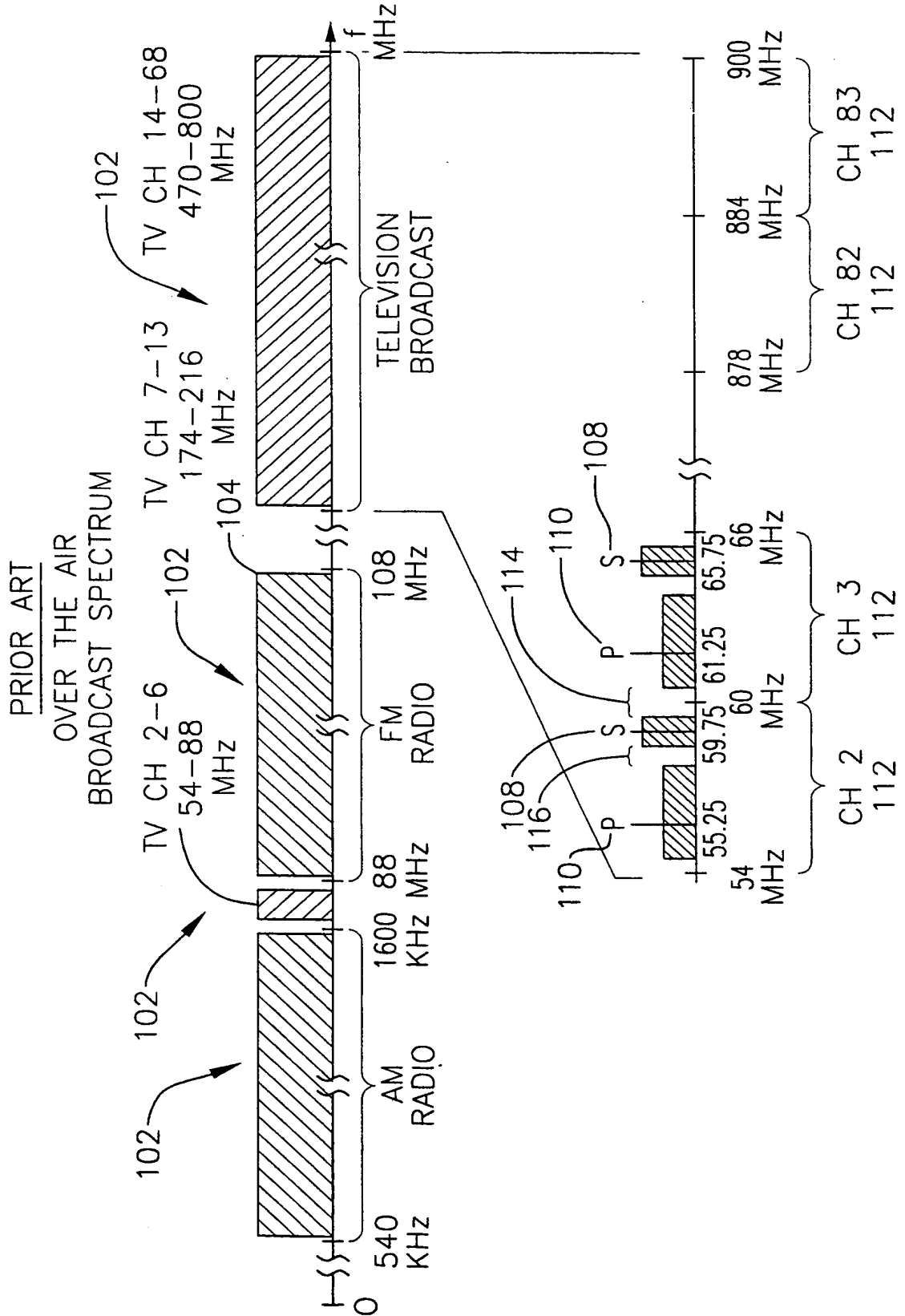


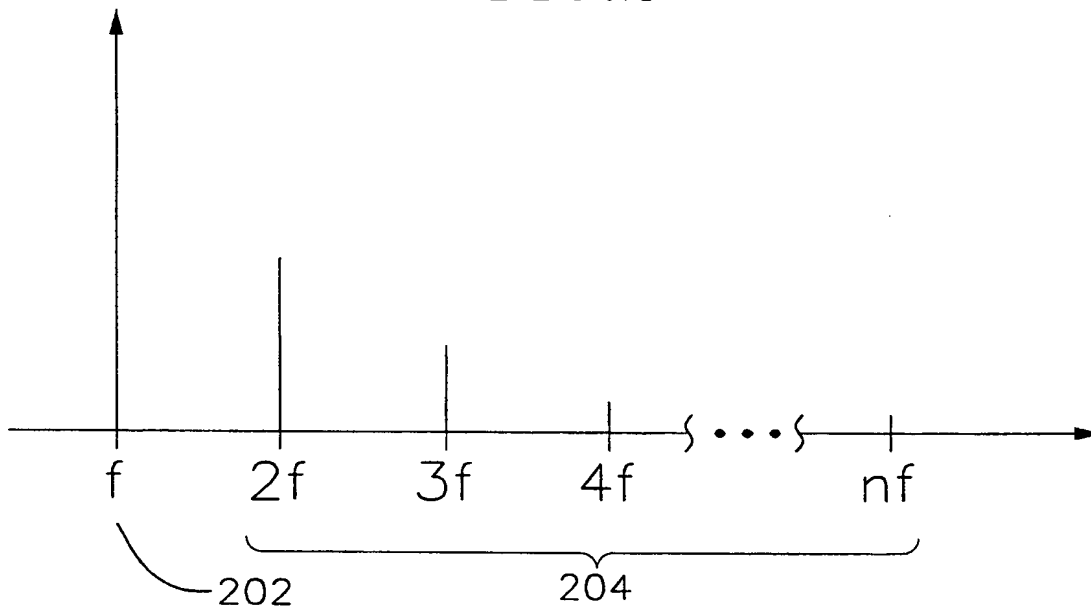


FIG. 1

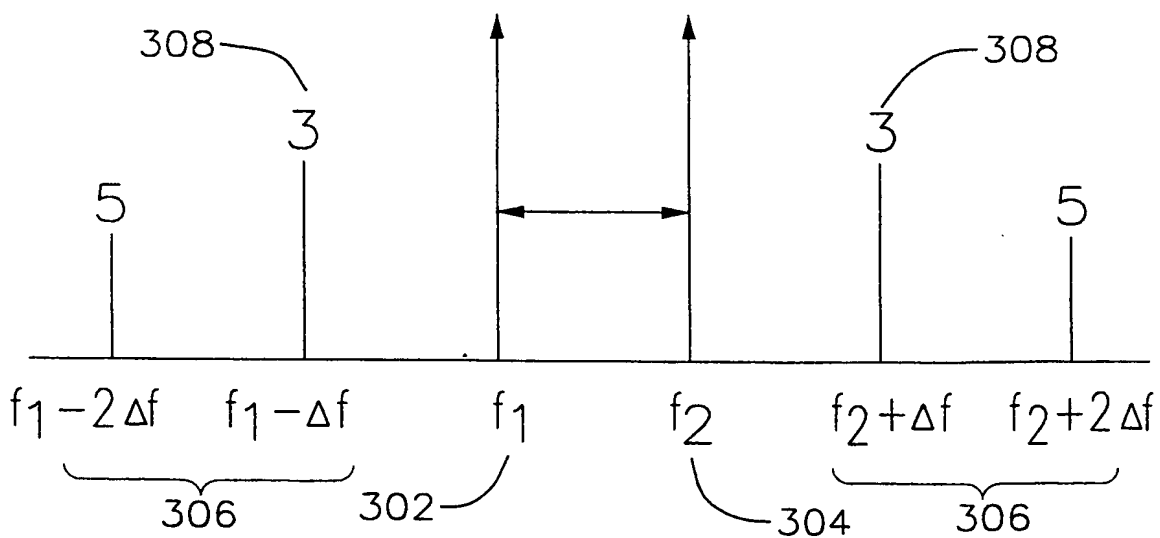




**FIG. 2**

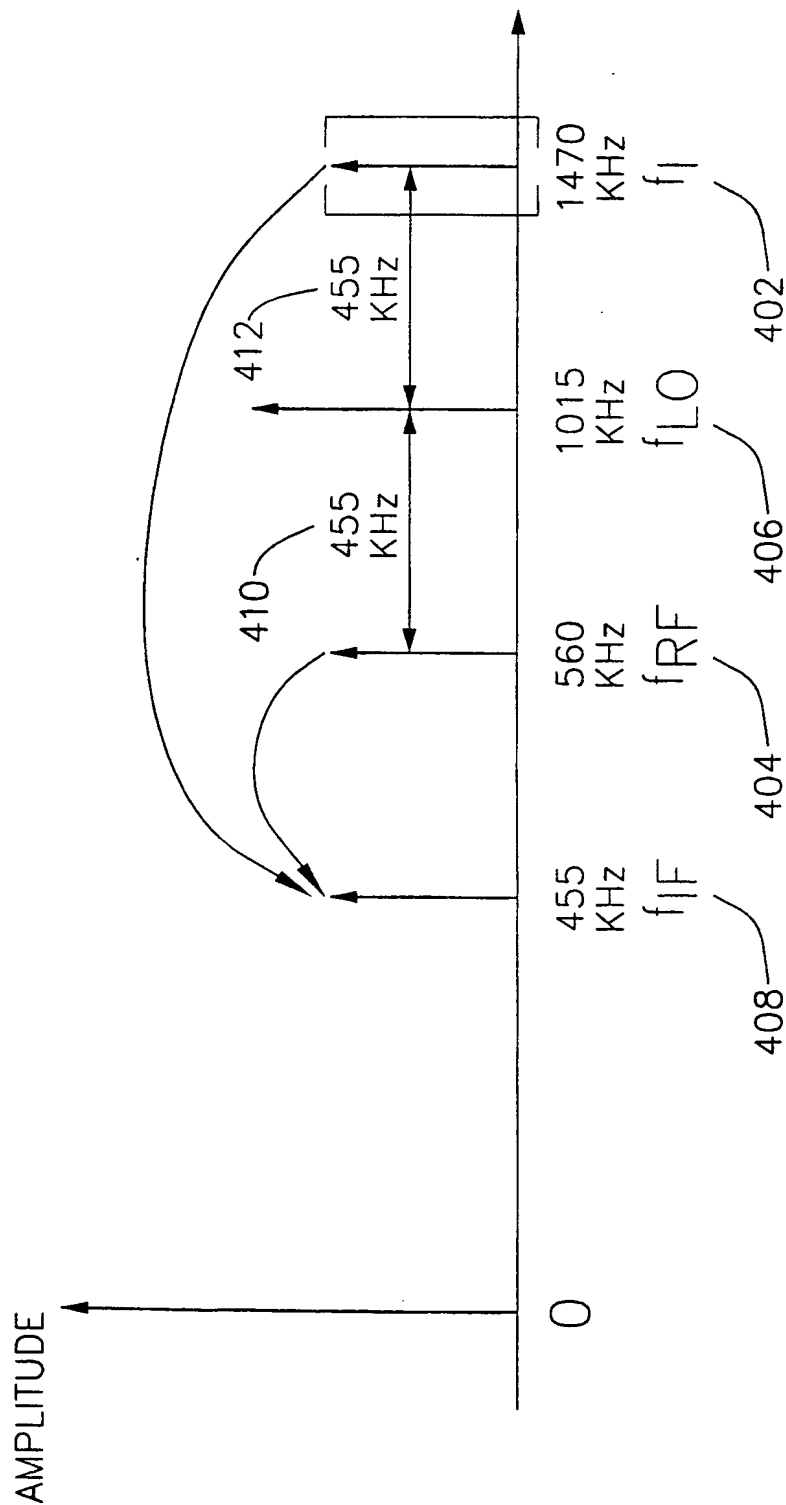


**FIG. 3**  
PRIOR ART



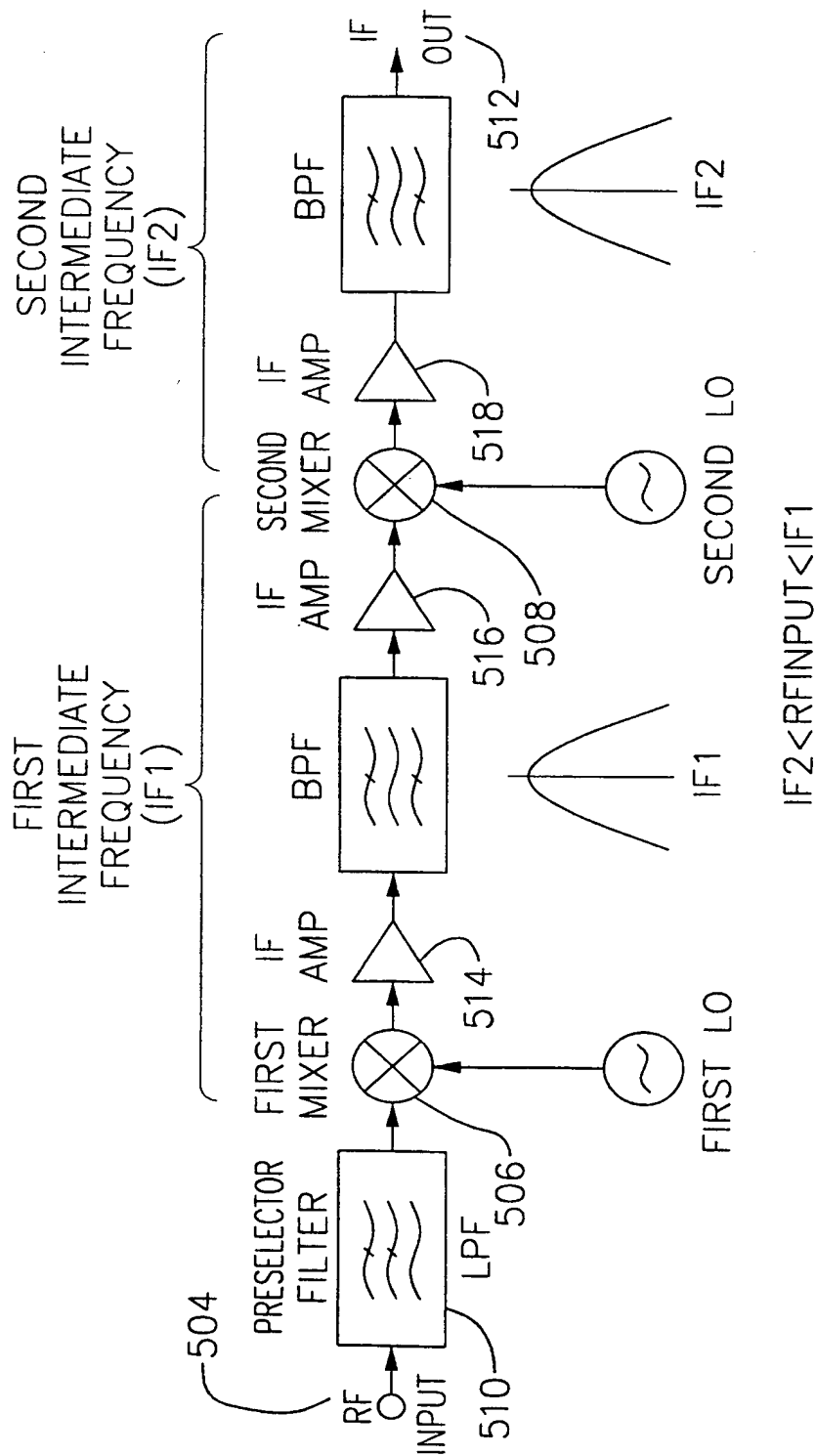


**FIG. 4**  
PRIOR ART



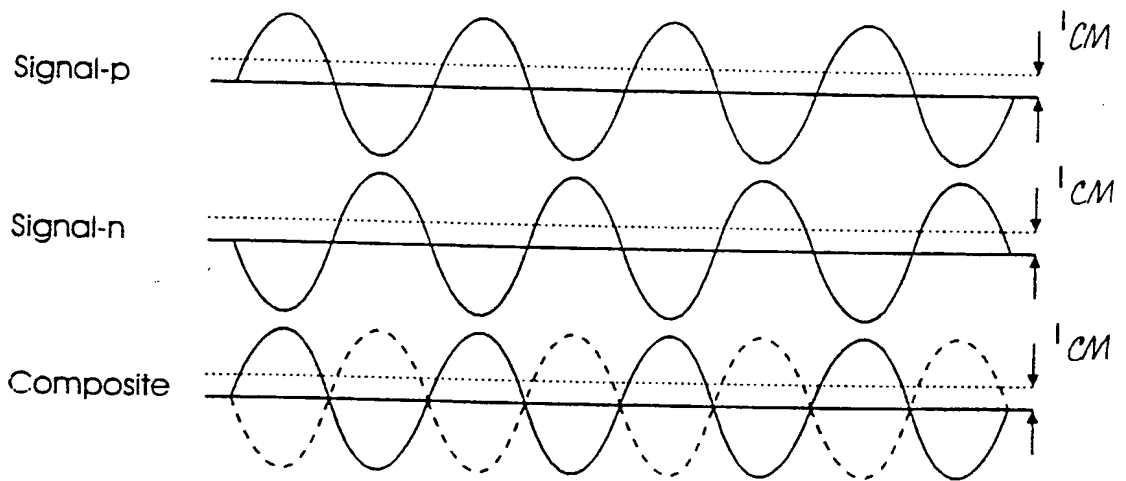


**FIG.5**  
 DUAL CONVERSION RECEIVER





**FIG. 6**



**FIG. 7**

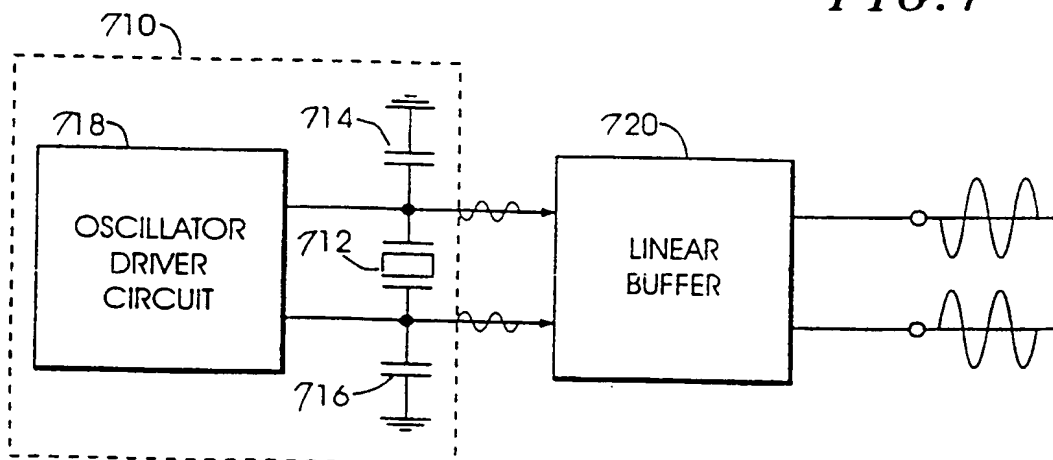




FIG. 8

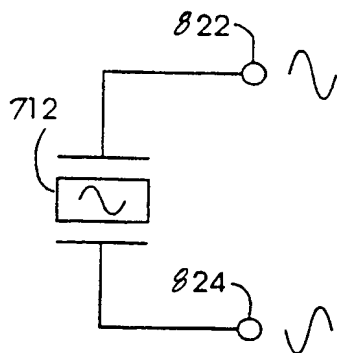


FIG. 9

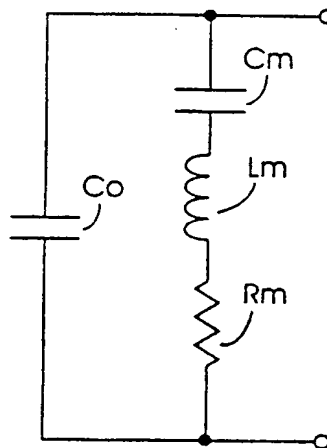


FIG. 10

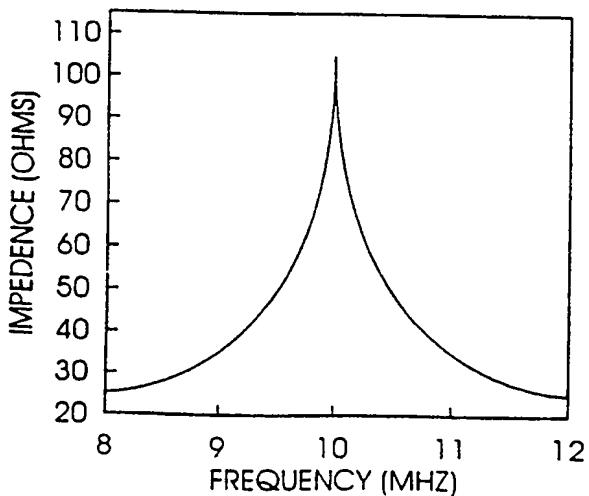


FIG. 11

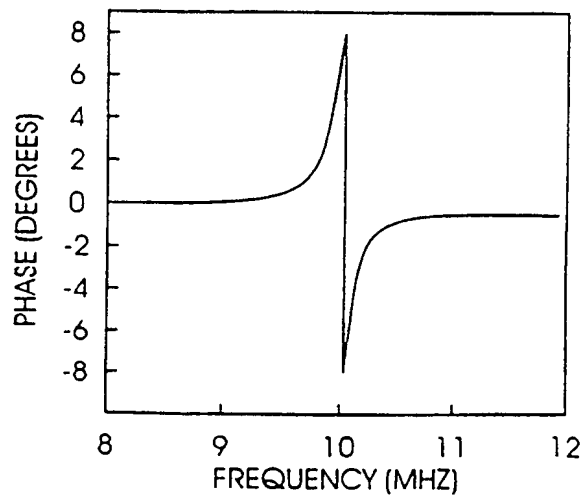




FIG. 12

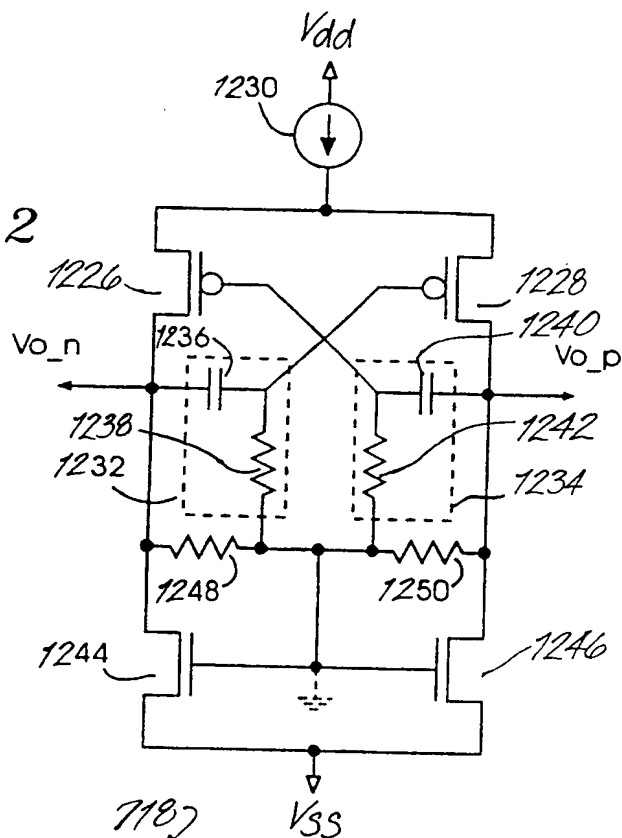


FIG. 13

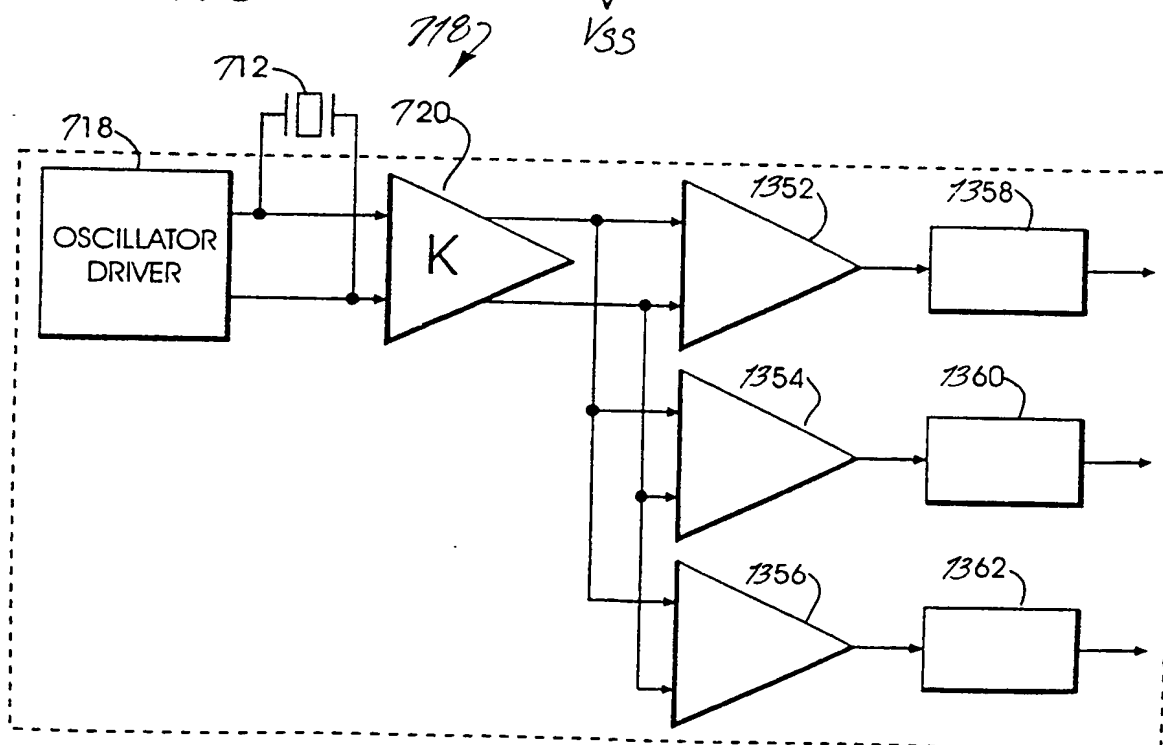
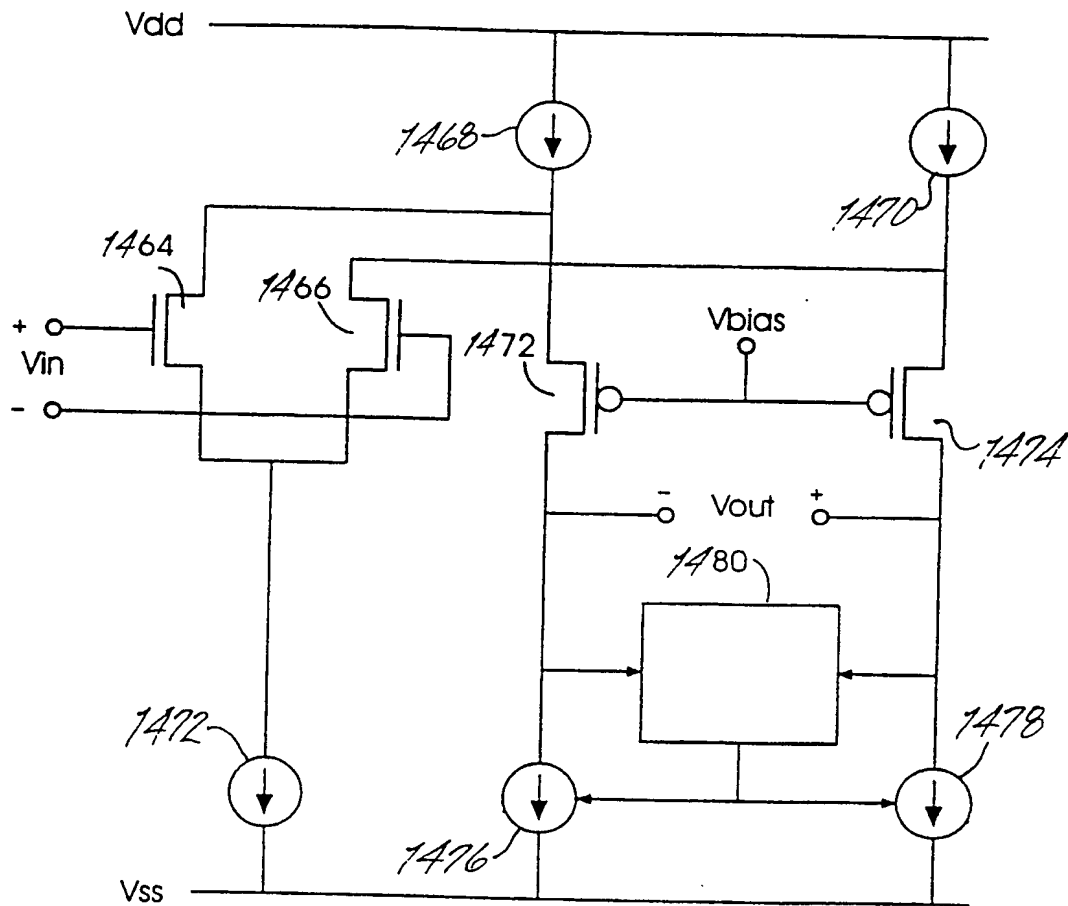




FIG. 14



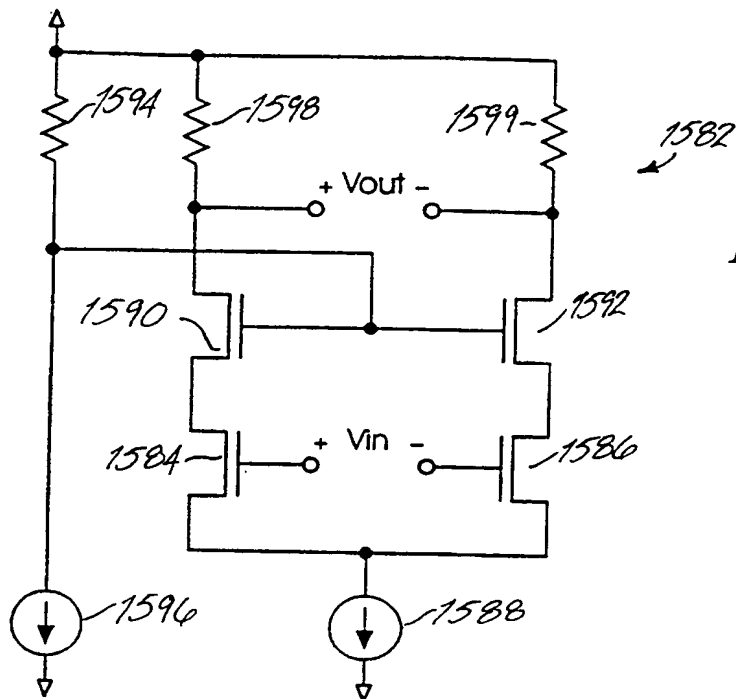
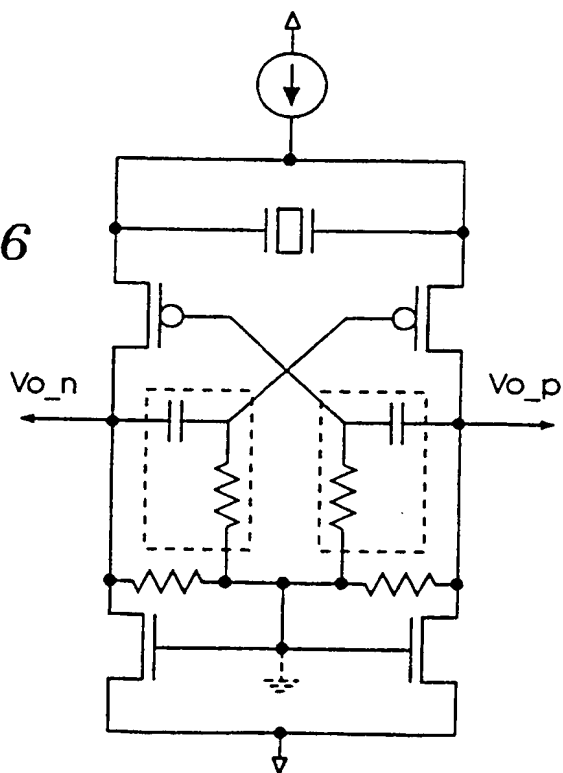


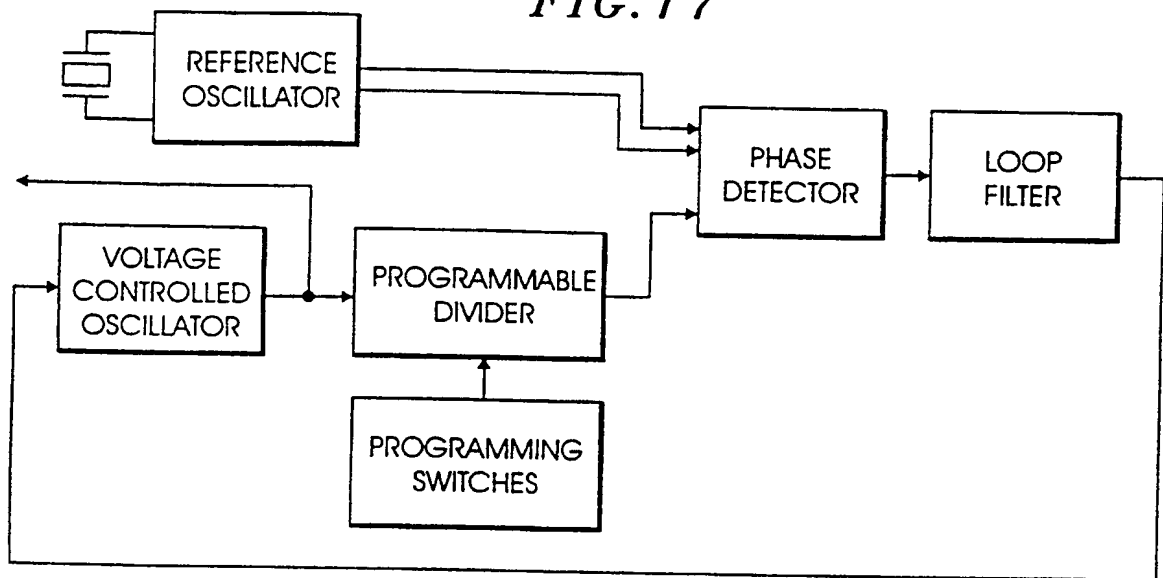
FIG. 15

FIG. 16





*FIG. 17*



*FIG. 18*

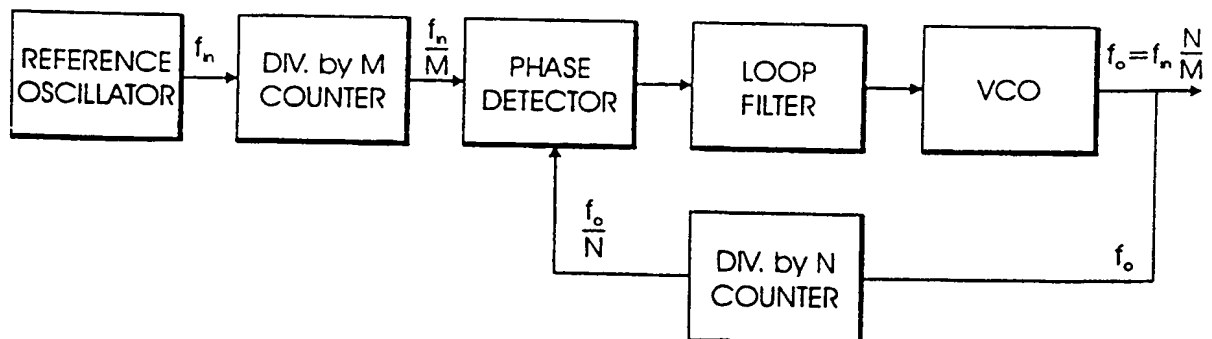
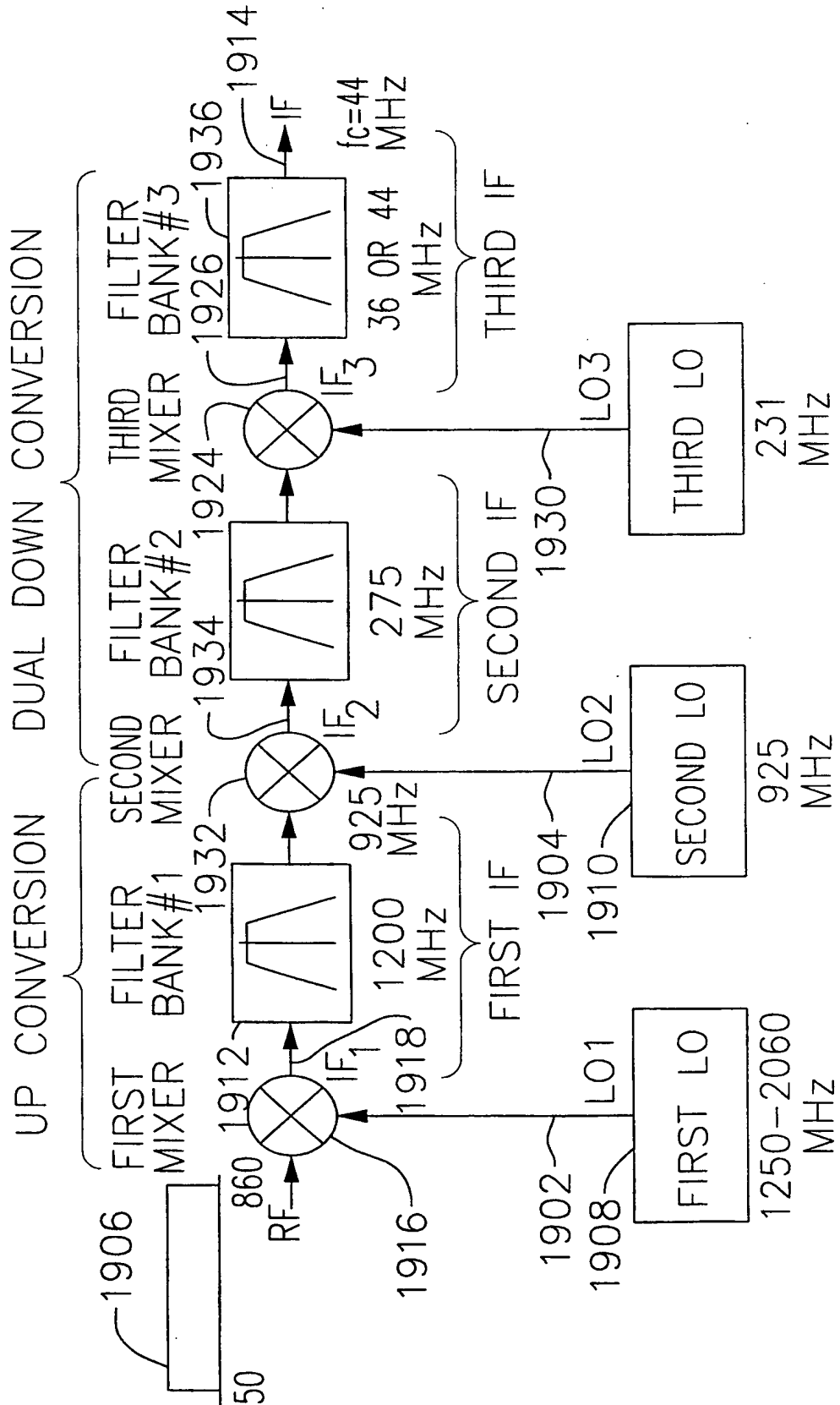




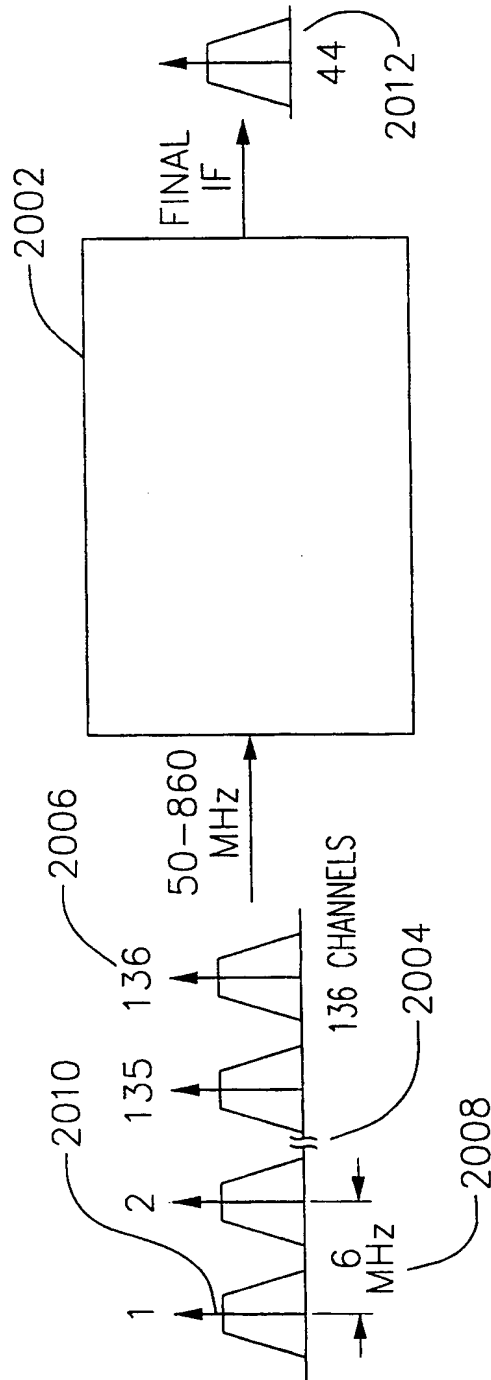
FIG. 19





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FIG. 20





# FIG. 21

PPL Xtol REFERENCE=10MHZ  
 LO-1, 10MHz FREQUENCY STEPS  
 LO-2, 100kHz FREQUENCY STEPS

44MHz IF

NOTE  
 • LO-2 REF=100KHz,  
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON  
 COARSE/FINE PLL SOLUTION:

IF1 (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2(MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102



# FIG.22

PPL X101 REFERENCE=10MHZ  
 LO-1, 10MHz FREQUENCY STEPS  
 LO-2, 100kHz FREQUENCY STEPS

36MHz IF

NOTE  
 $\frac{LO-2}{\bullet LO-2}$  REF=100KHz,  
 SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON  
 COARSE/FINE PLL SOLUTION:

Frq (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0



**FIG.23**

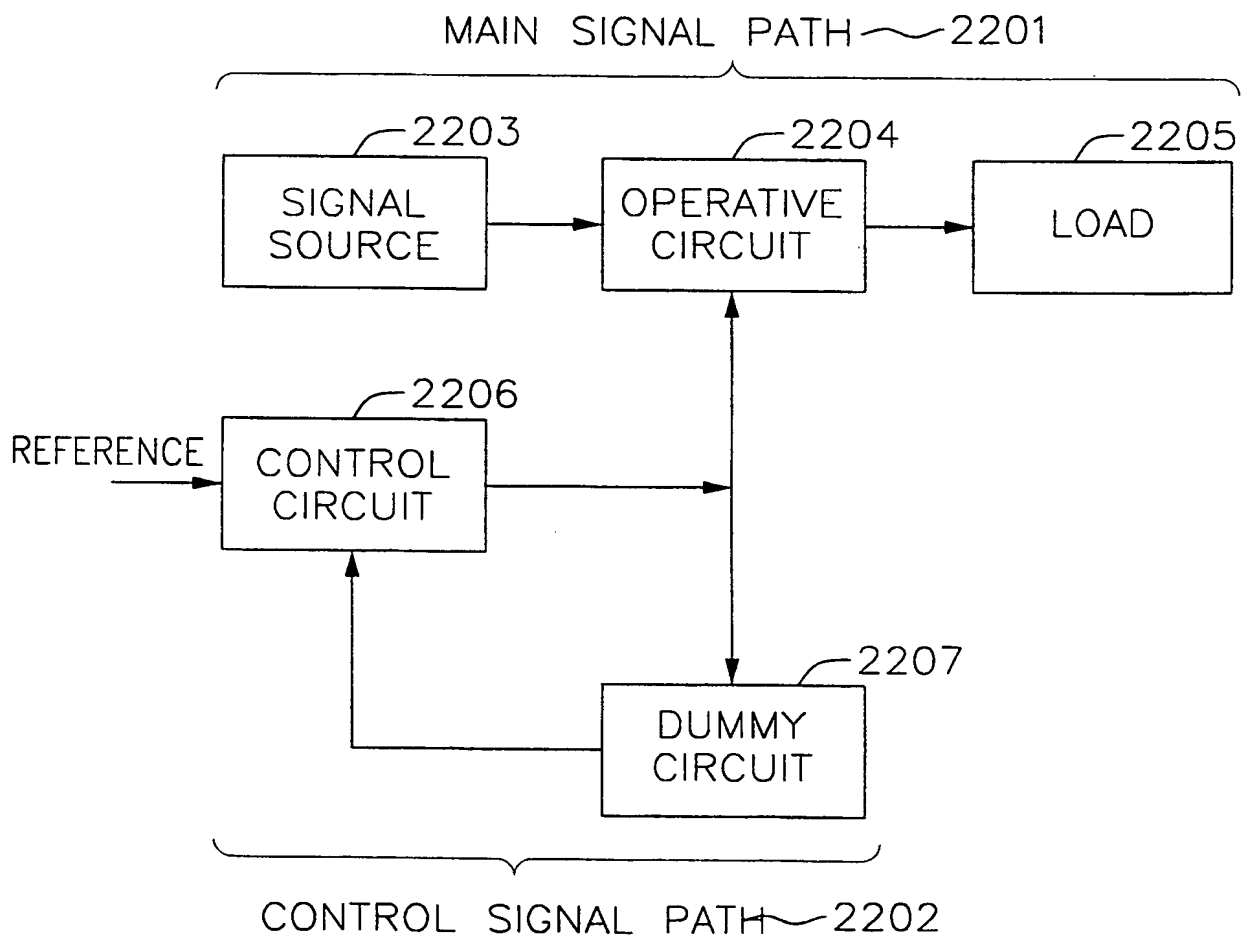




FIG. 24a

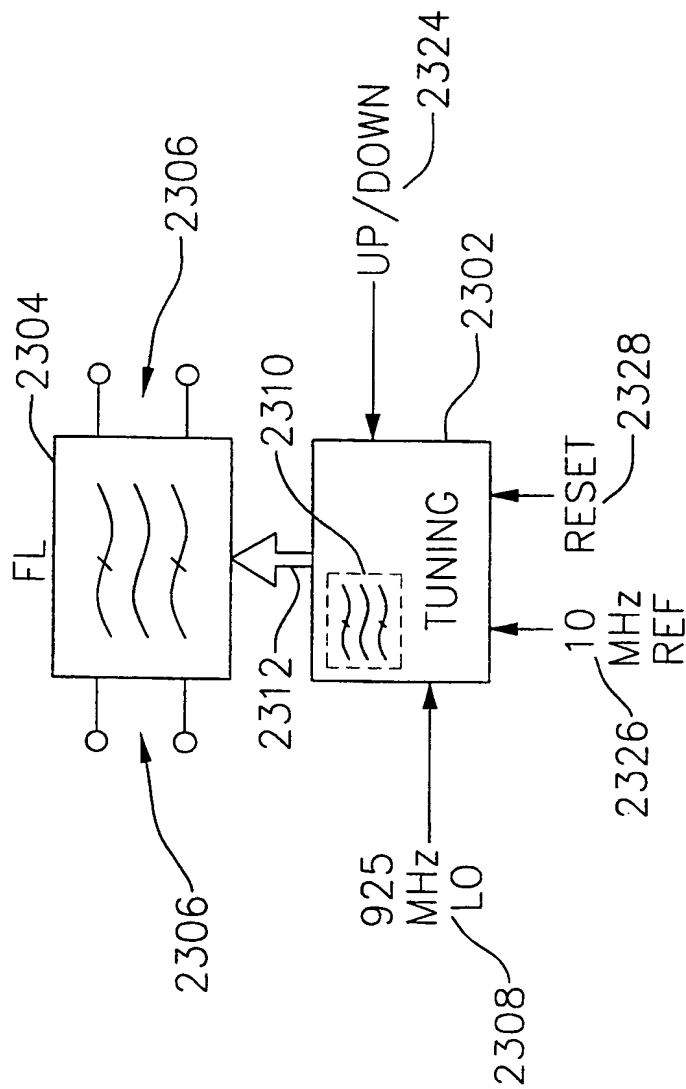




FIG. 24b

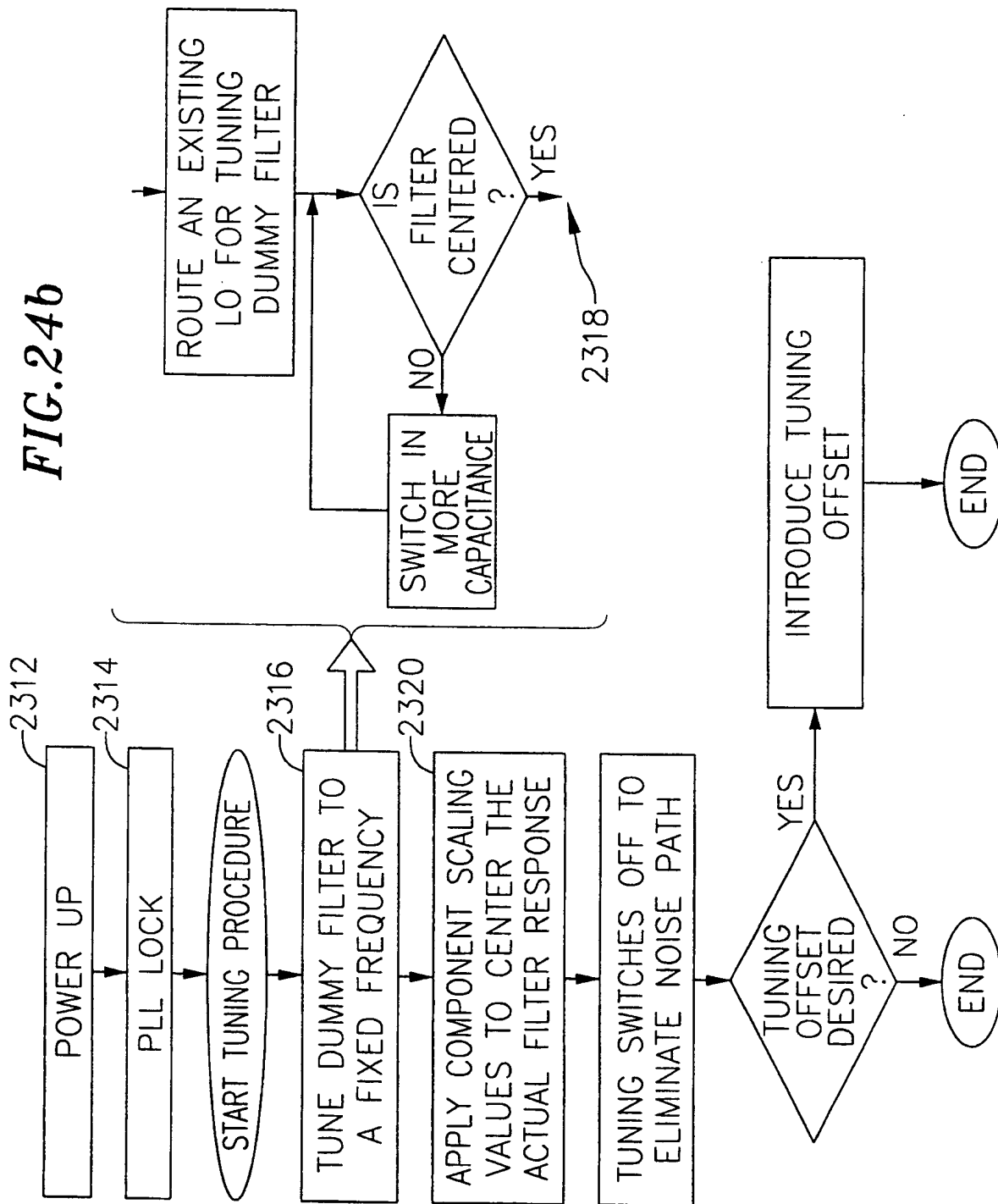




FIG. 24c

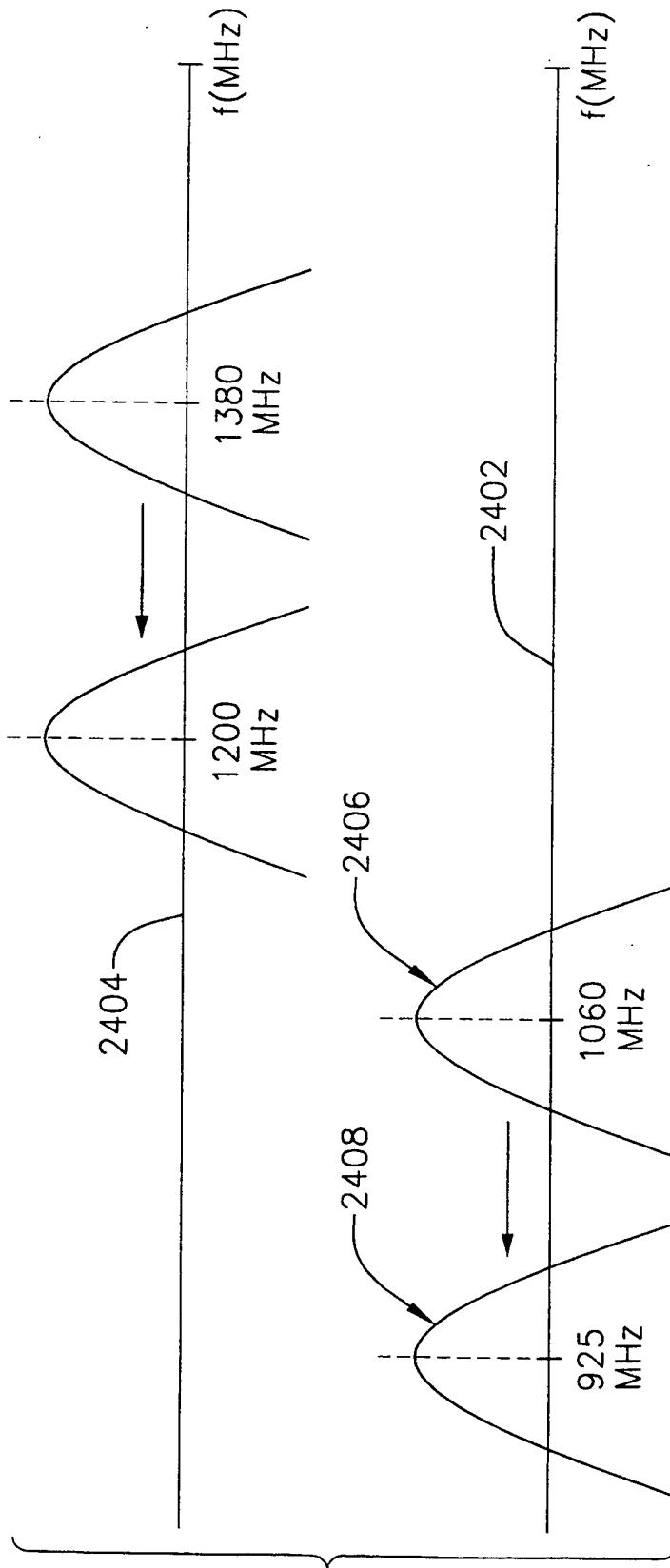
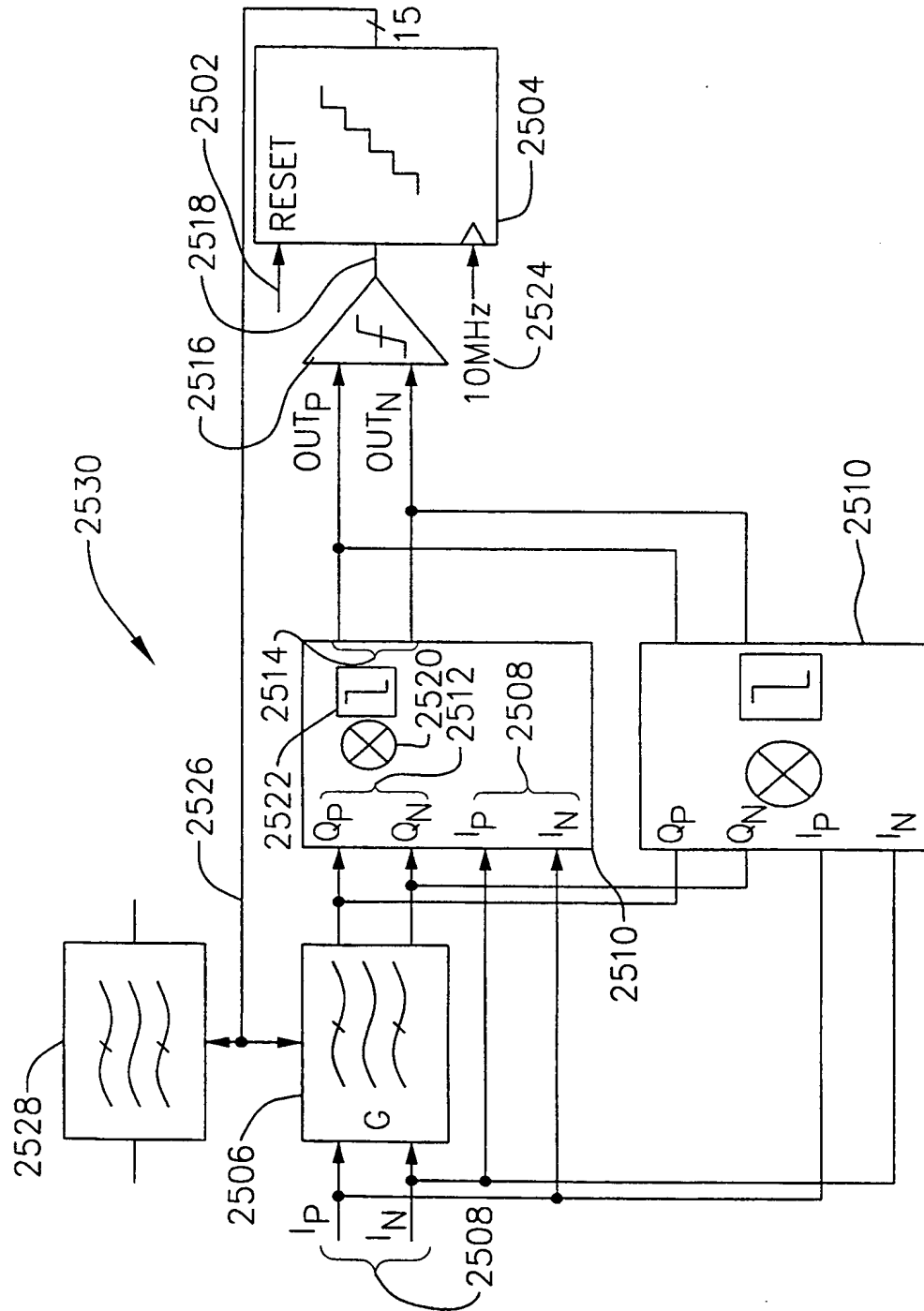


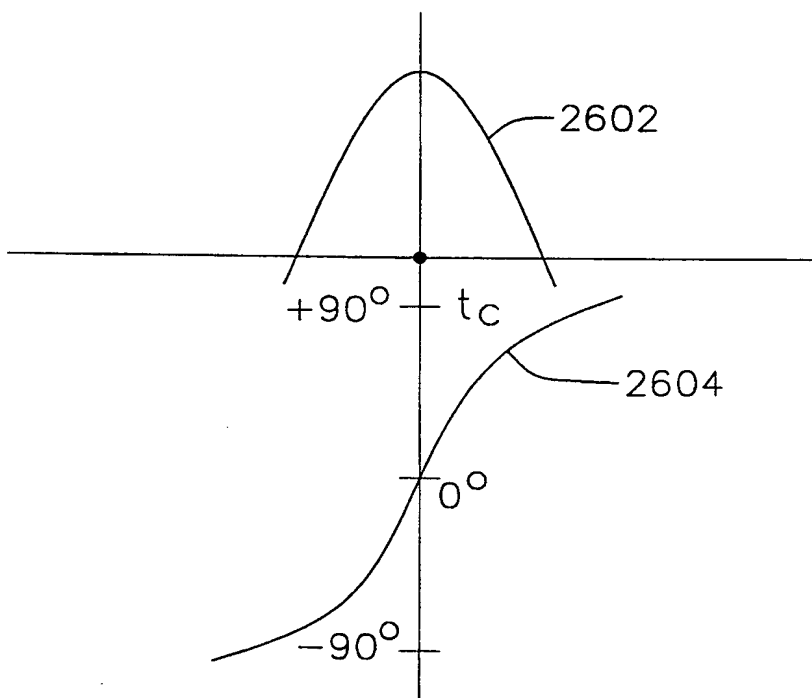


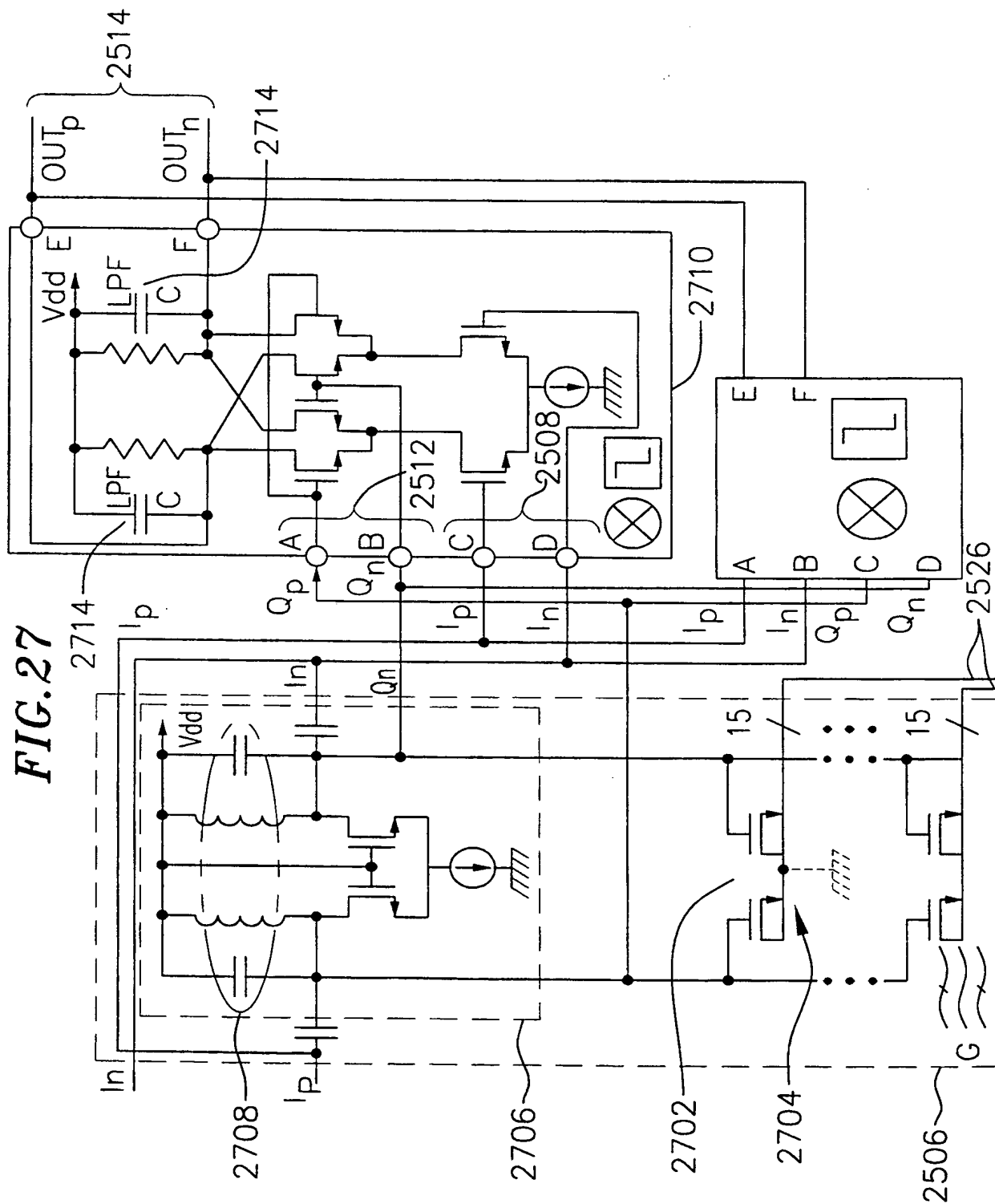
FIG. 25





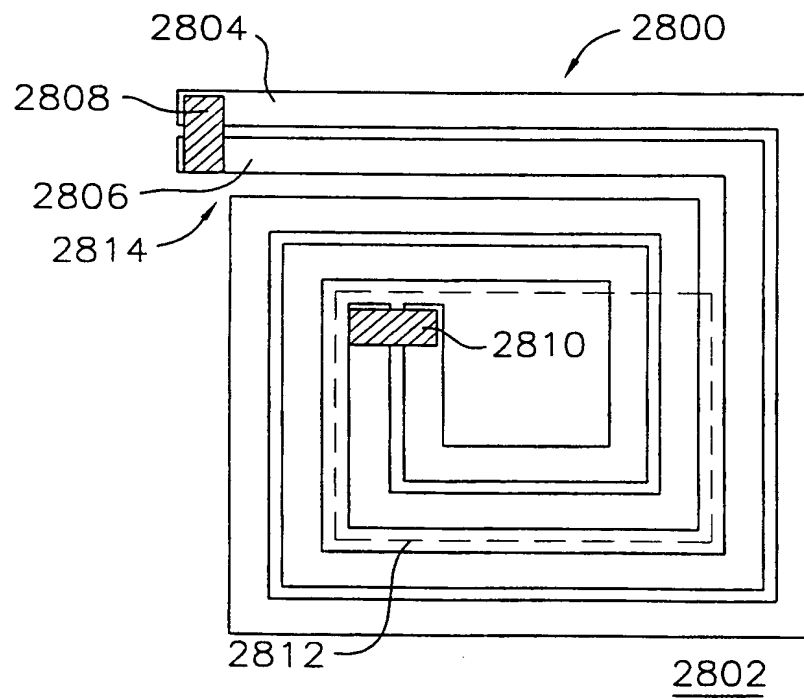
**FIG.26**





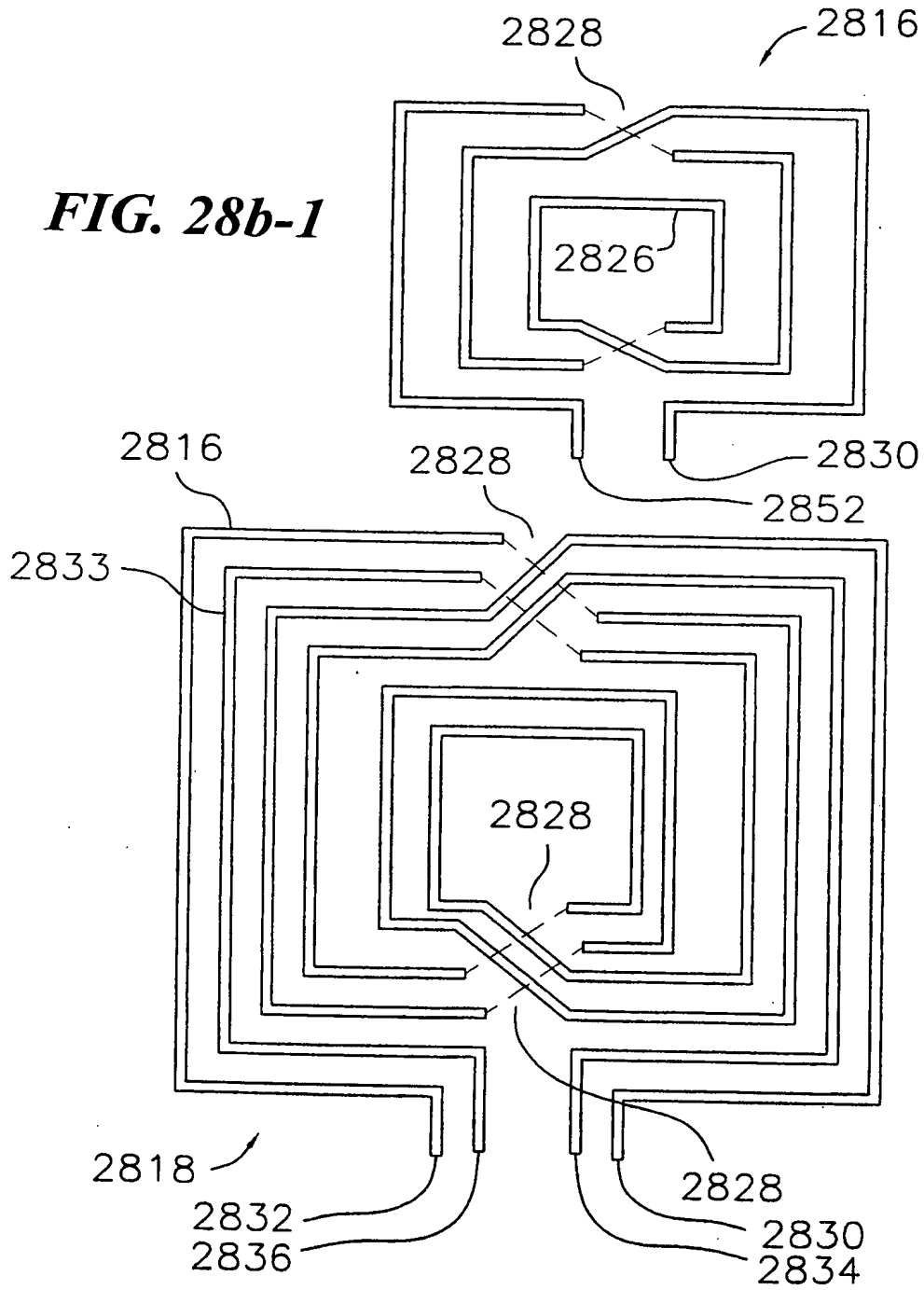


*FIG. 28a*



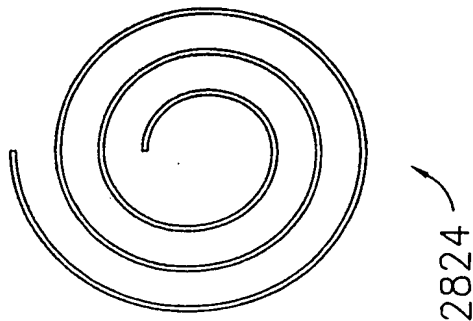


**FIG. 28b-1**

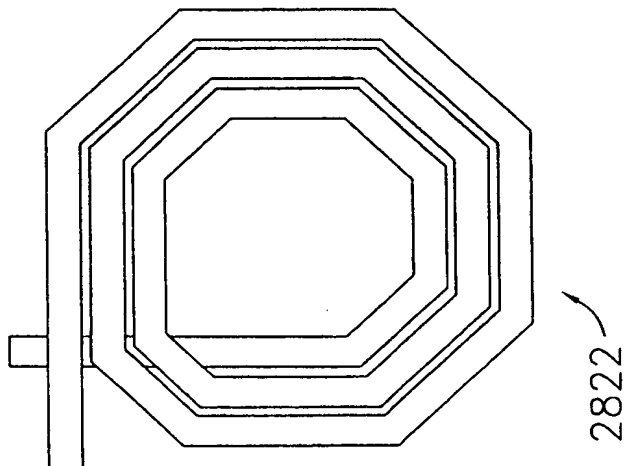




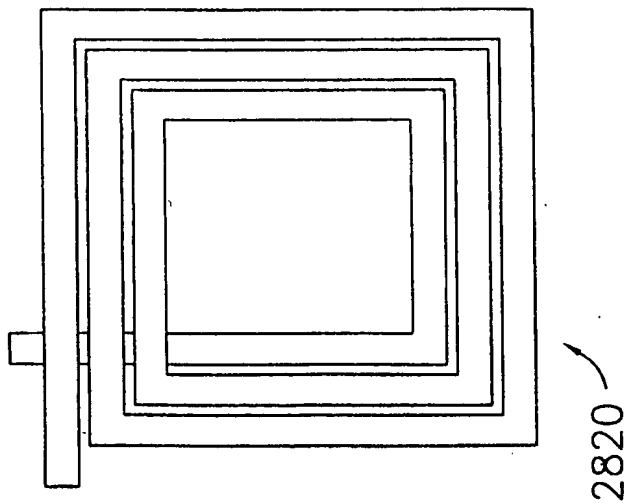
**FIG. 28b-4**



**FIG. 28b-3**

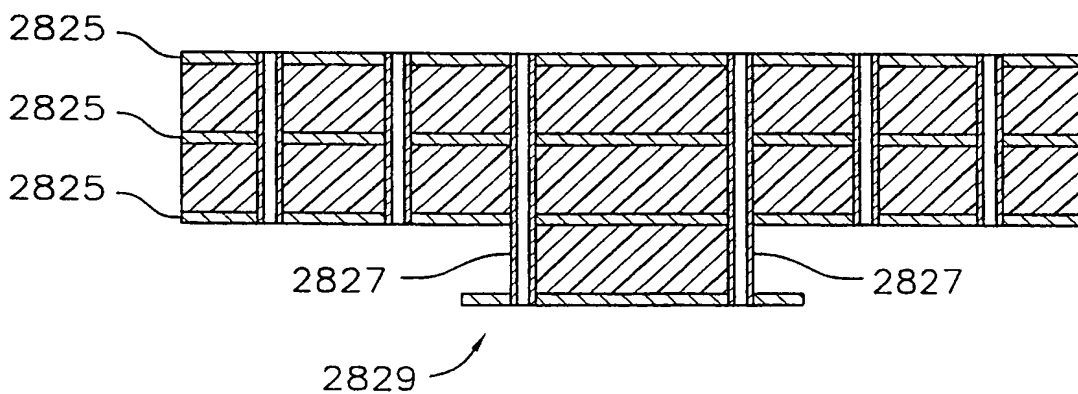


**FIG. 28b-2**

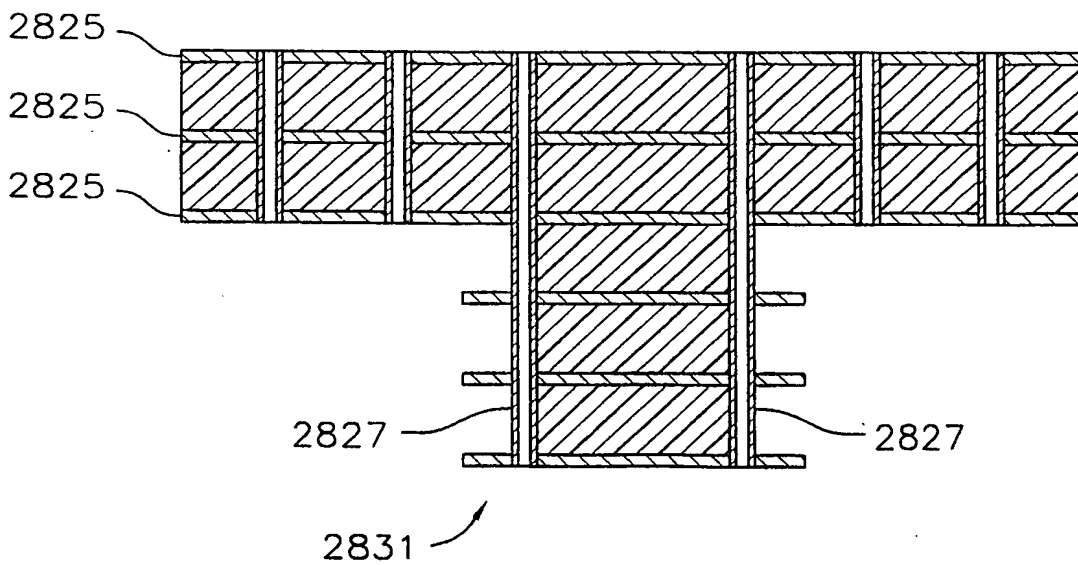




**FIG. 28b-5**

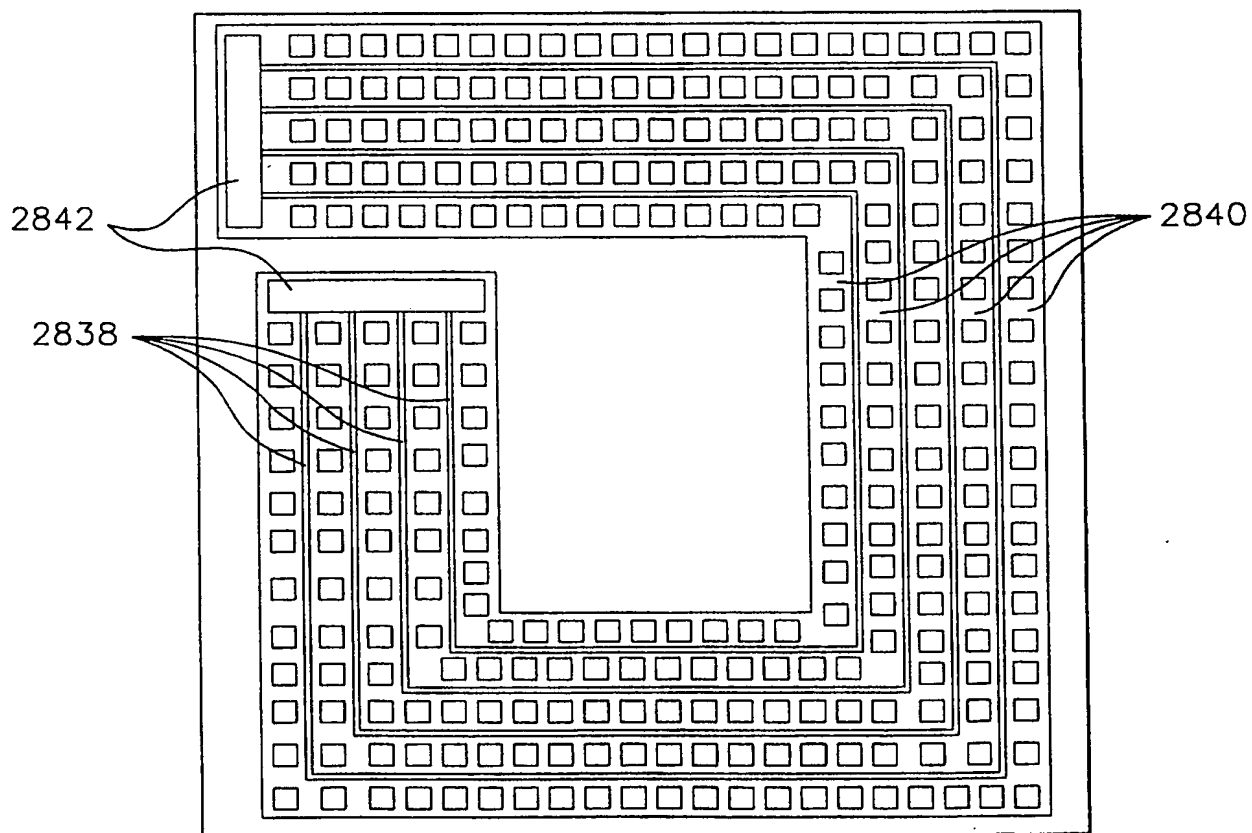


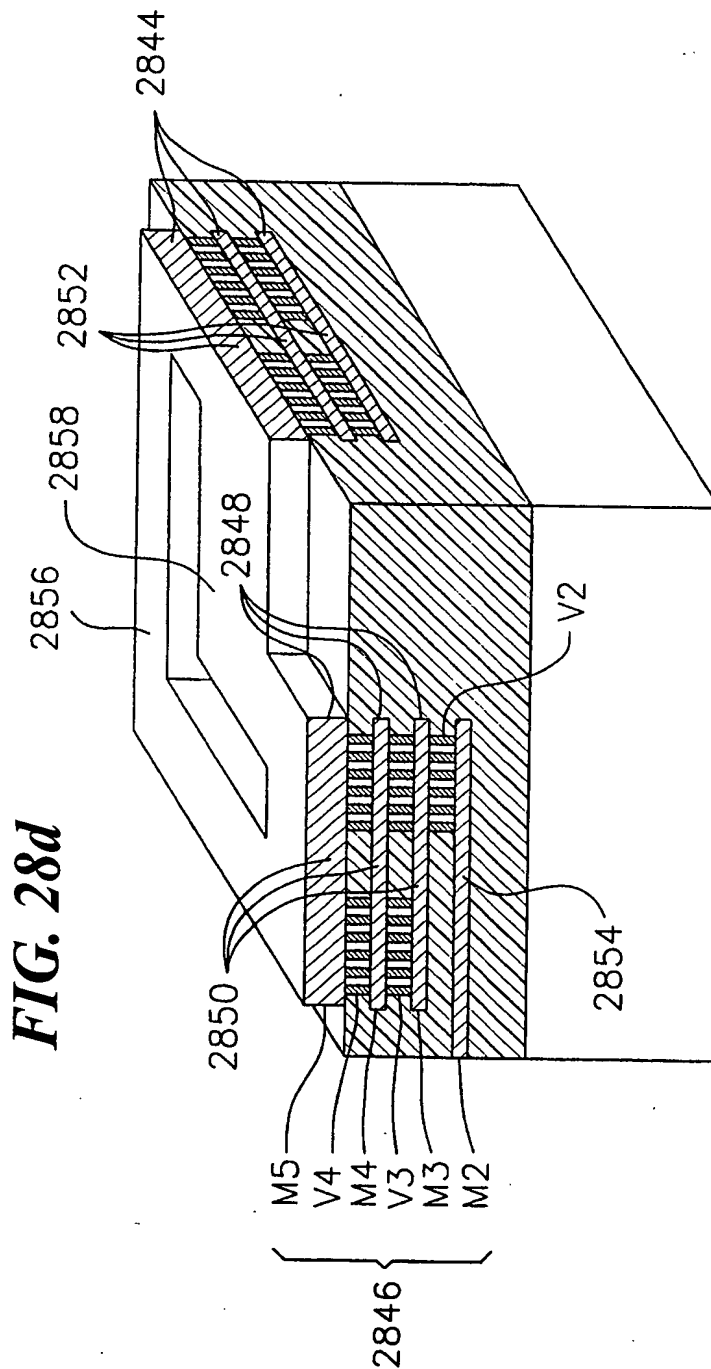
**FIG. 28b-6**





**FIG. 28c**

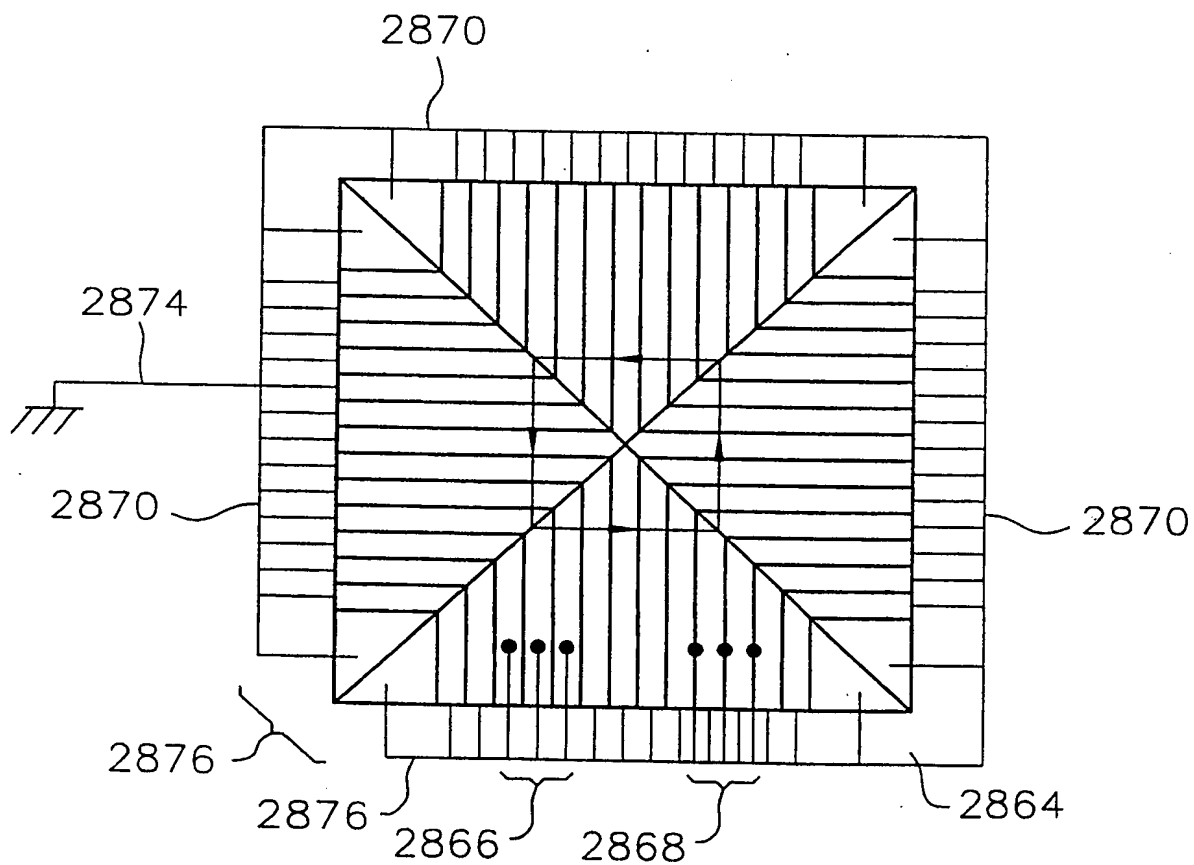




Sheet 28 of 69  
Appl. No. 09/493,942; Filed: Jan 28, 2000  
Dkt No. 1875.1380006; Group Unit: 2832  
Inventor: James Y.C. Chang Tel: 202-371-2600  
Title: Multi-Track Integrated Spiral Inductor



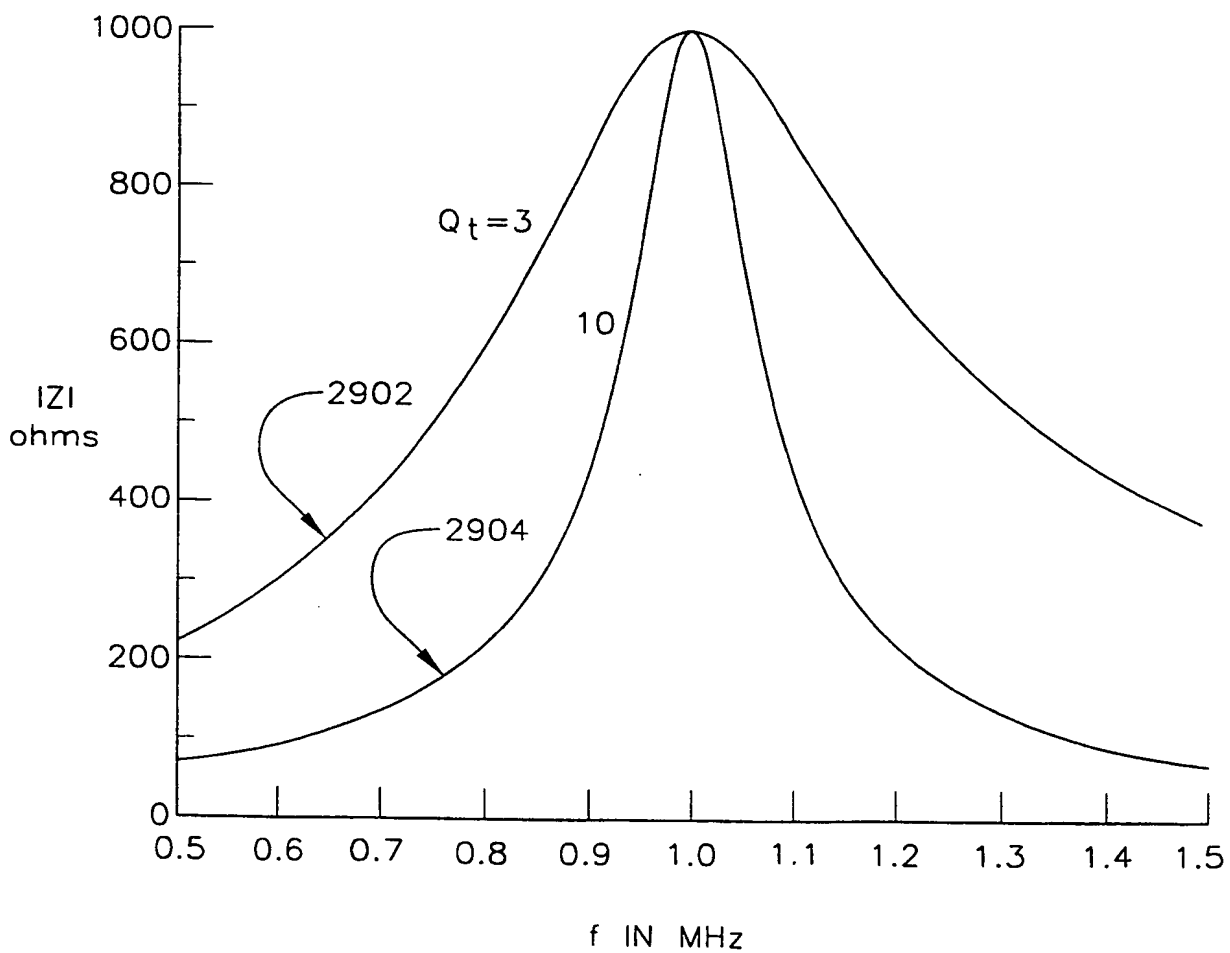
**FIG. 28f**





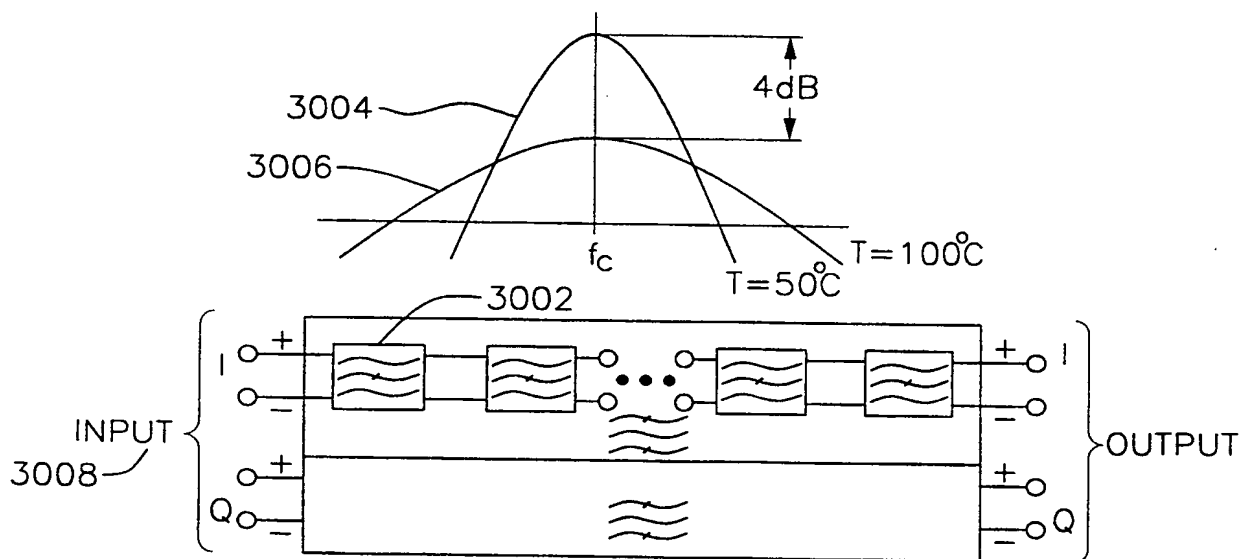
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*FIG.29*





**FIG.30**



**FIG.31**

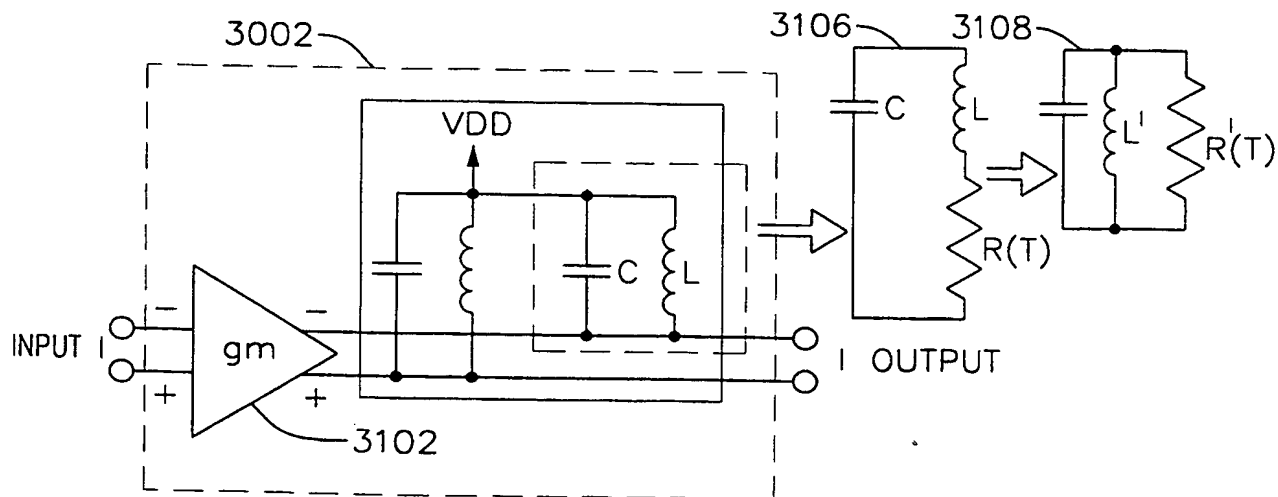




FIG. 32

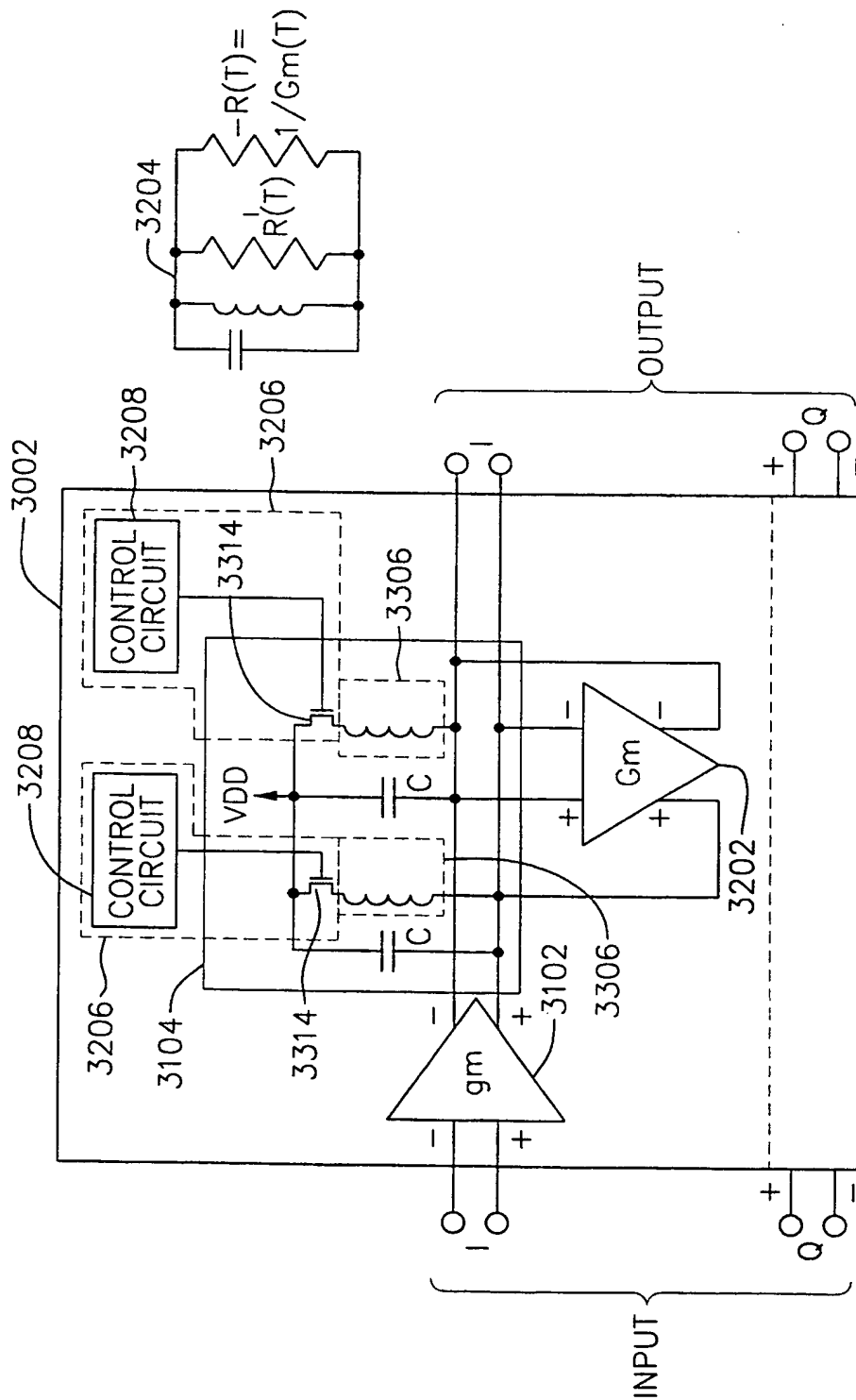
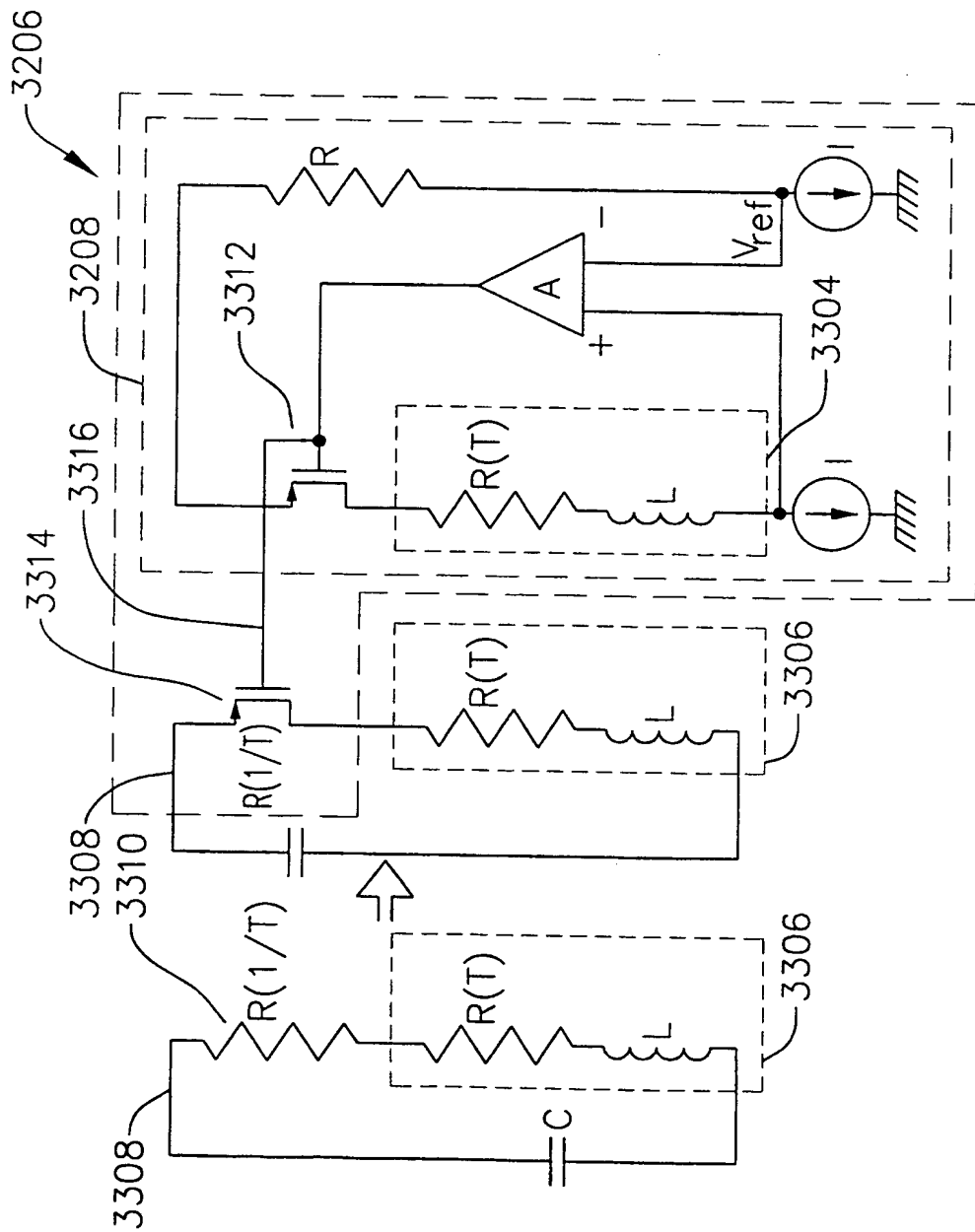


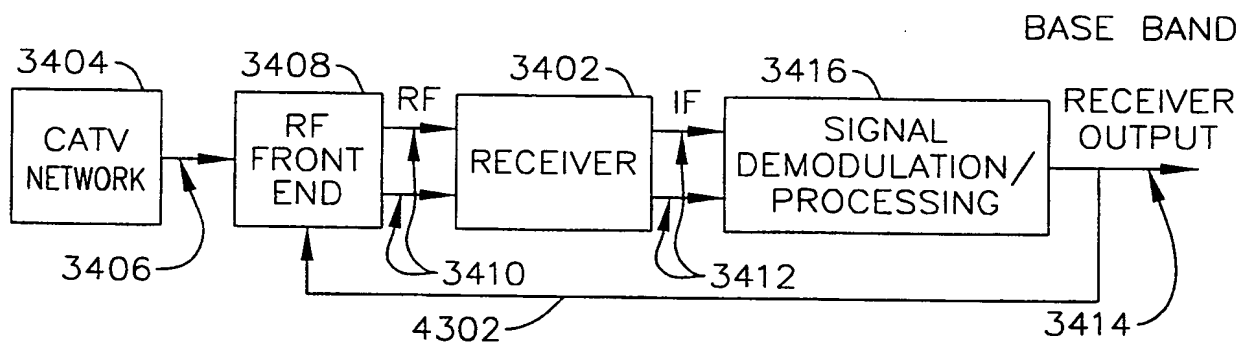


FIG. 33





**FIG.34**



**FIG.35**

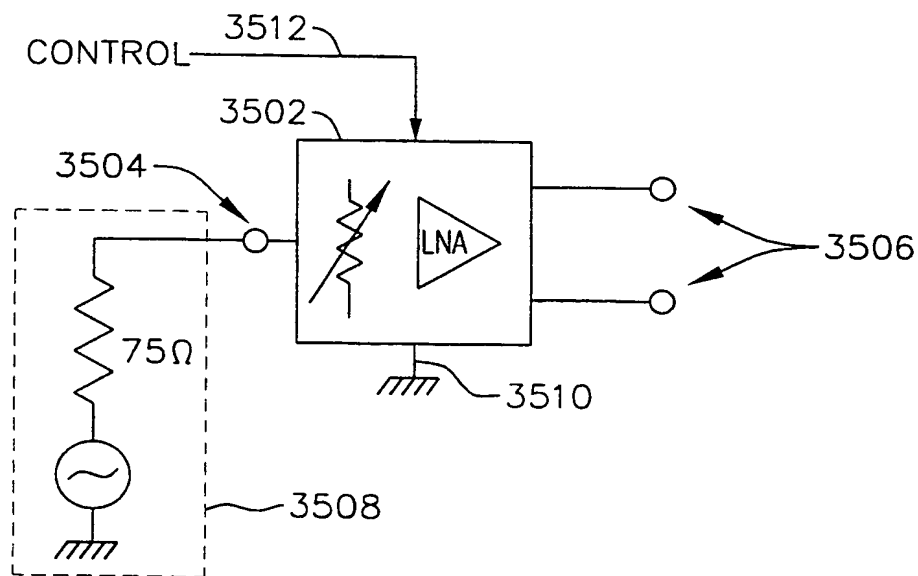






FIG. 37

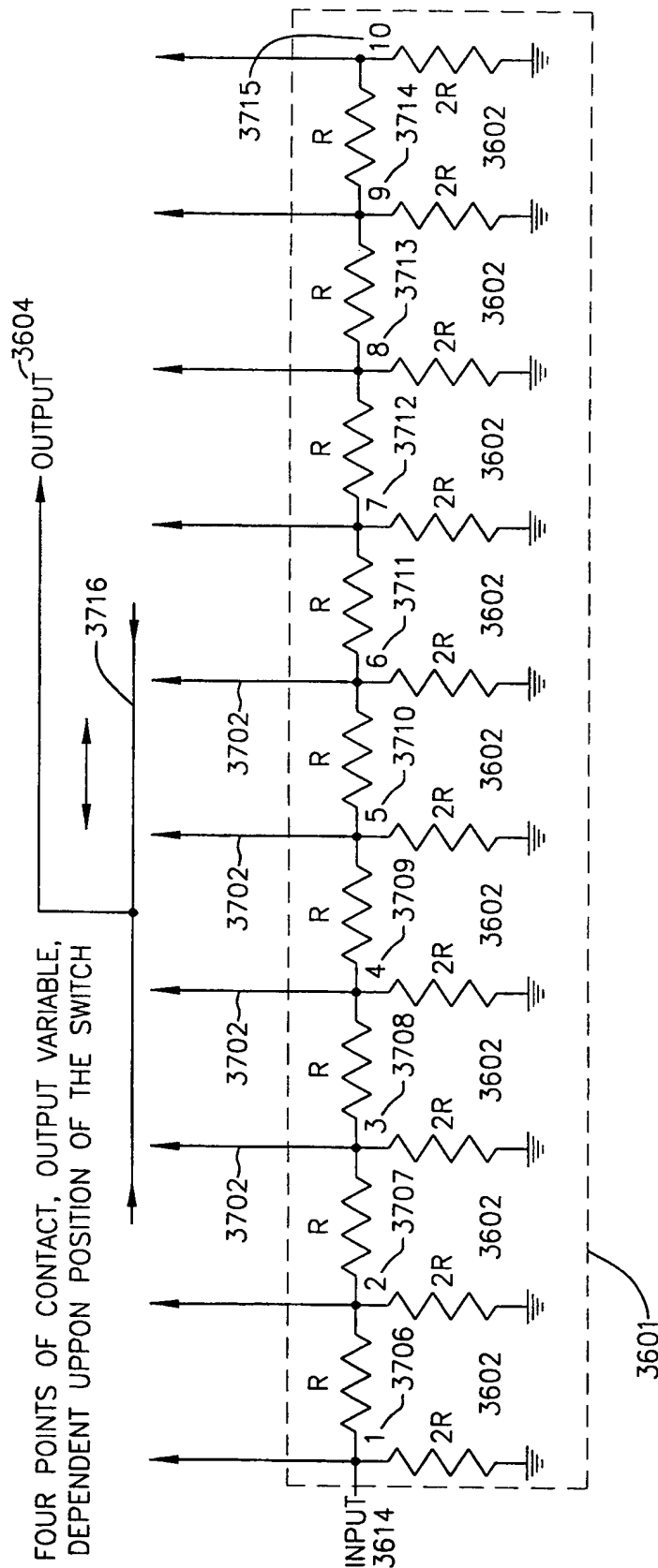




FIG. 38

PGA SETTINGS

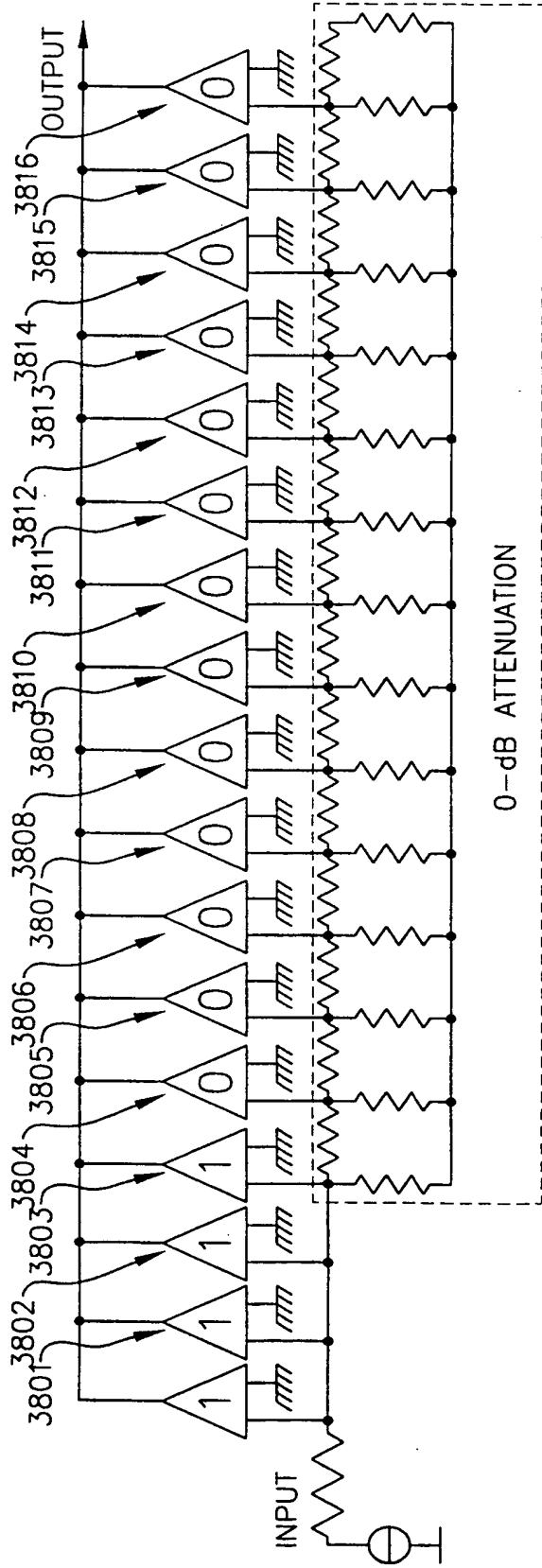




FIG. 39

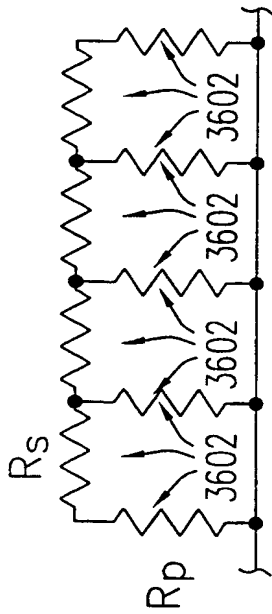


FIG. 40

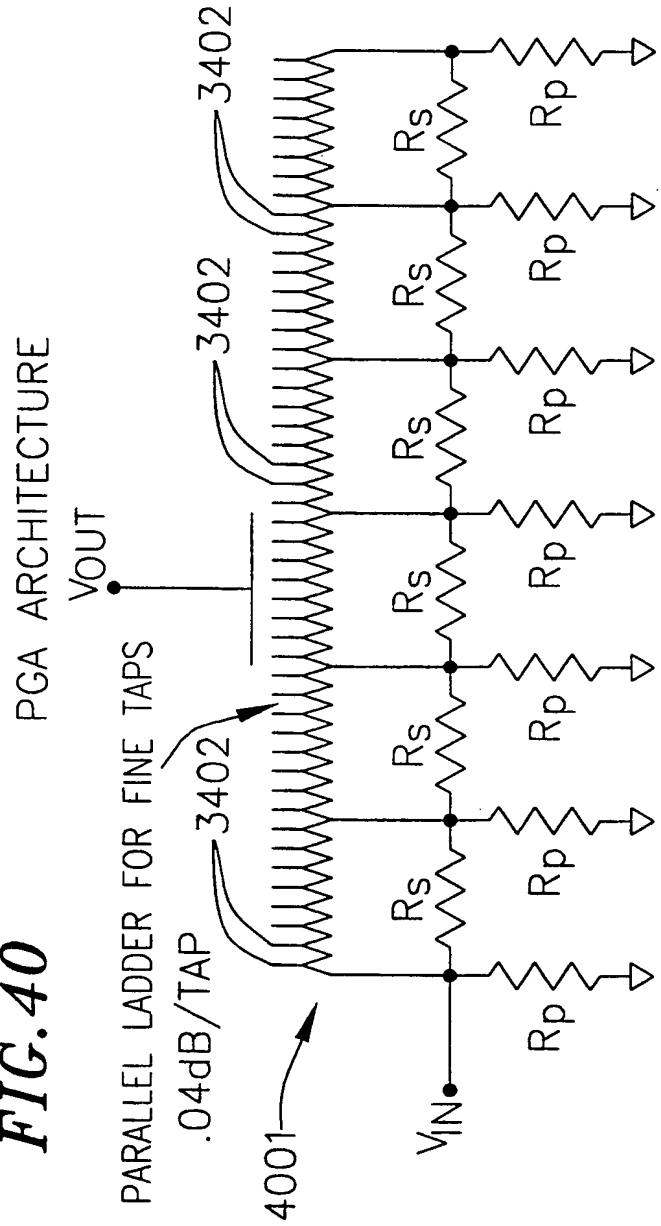




FIG. 41

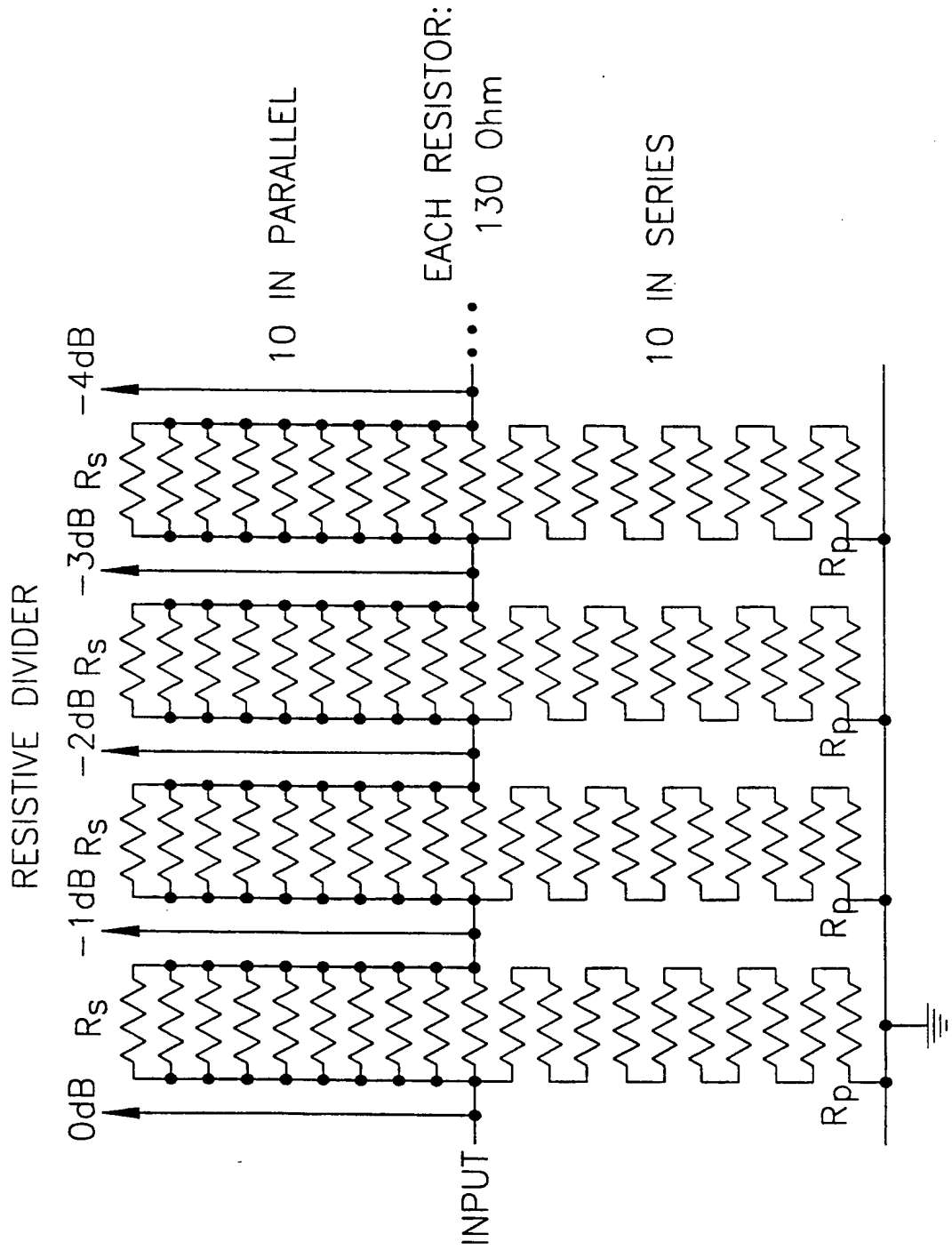
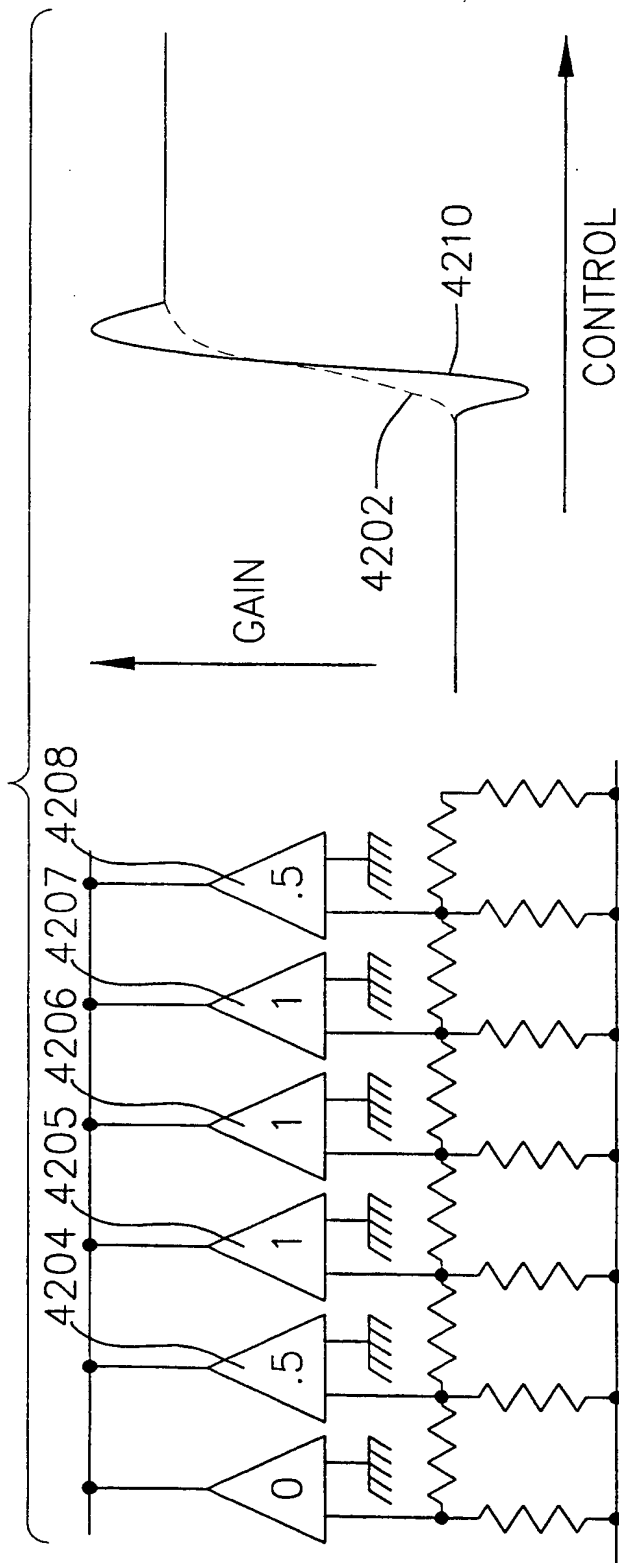




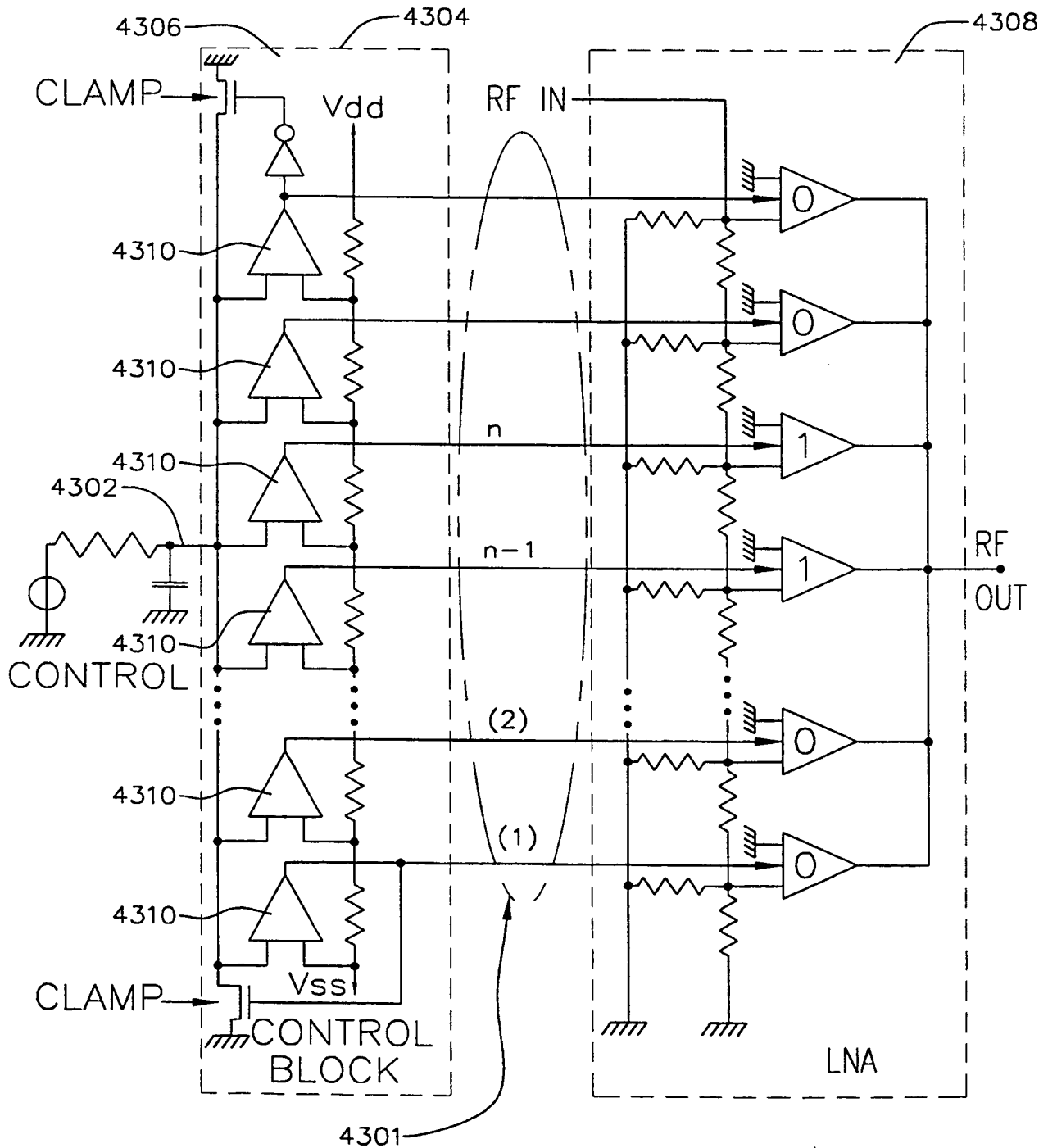
FIG. 42

NON-MONOTONICITY





**FIG. 43**  
CLAMPING CONTROL RANGE





**FIG. 44a**  
CONTROLLED GAIN COMPARATOR

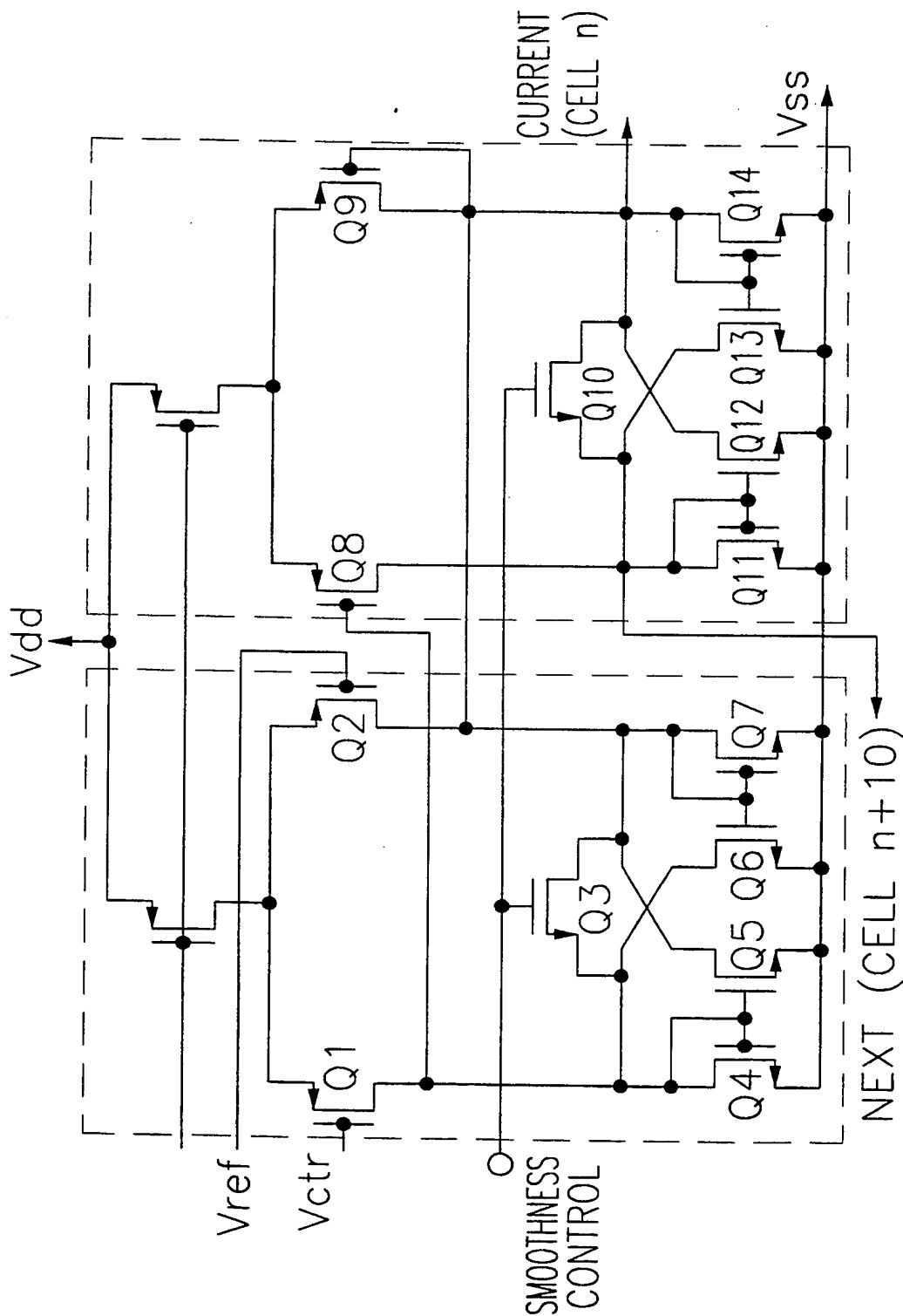




FIG. 44b

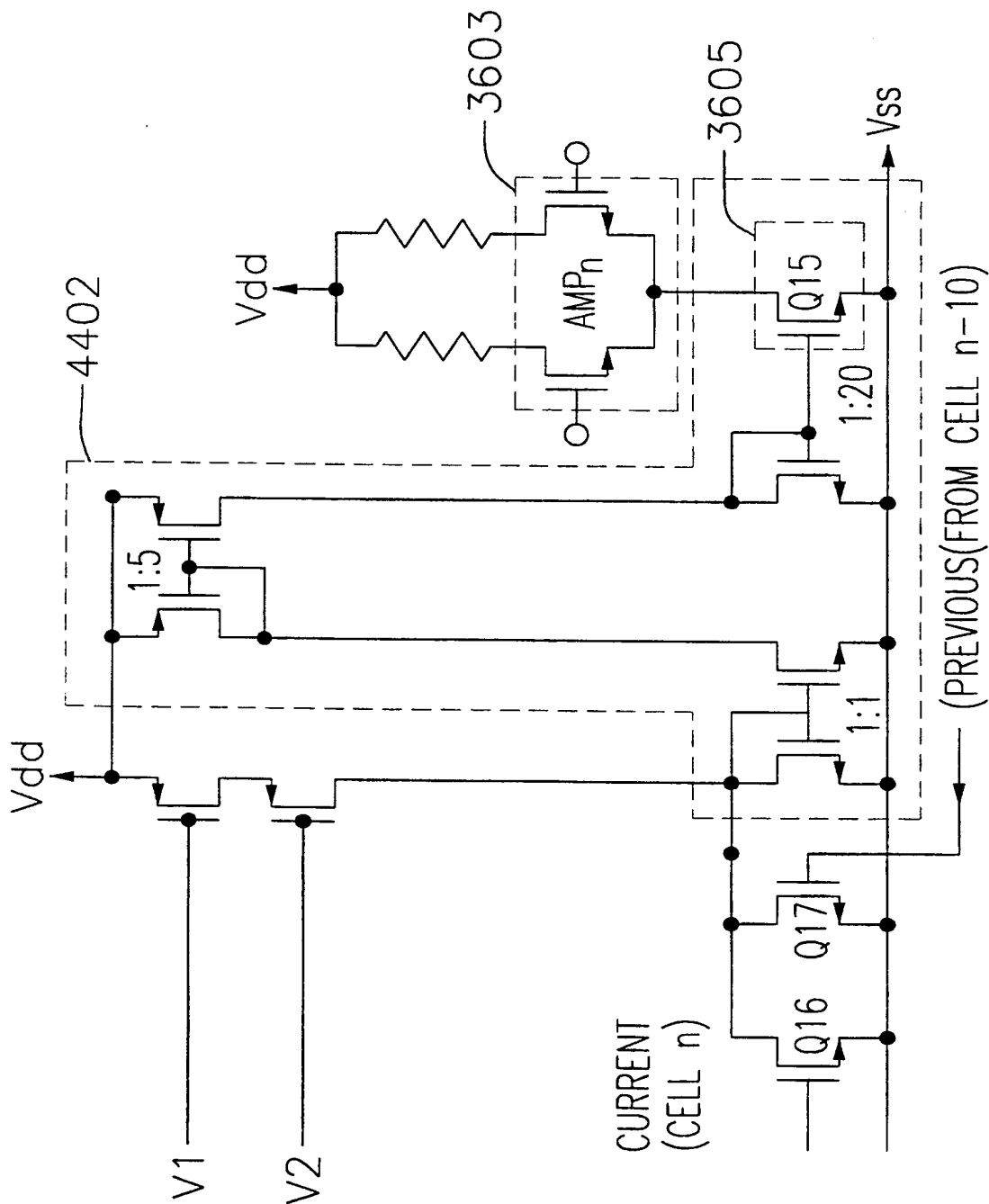
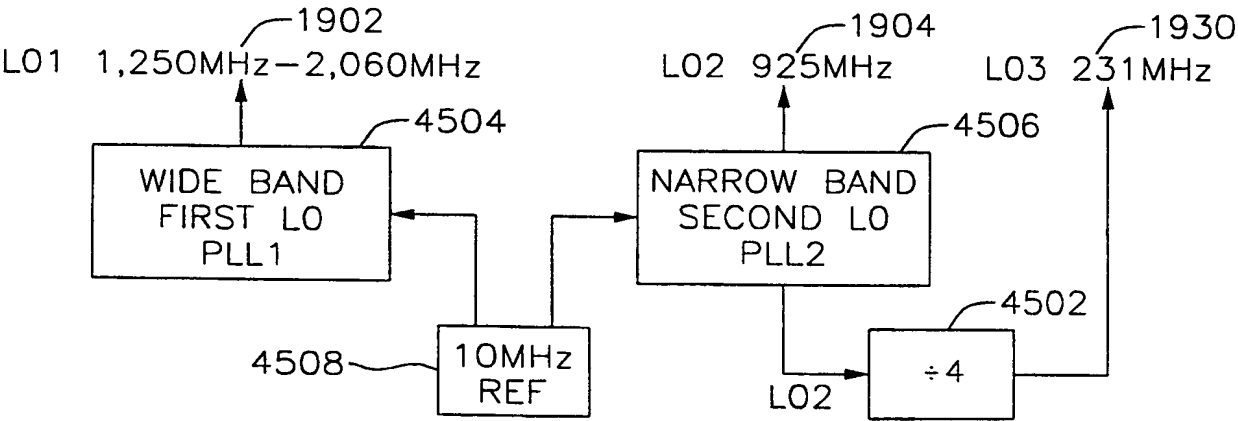




FIG. 45



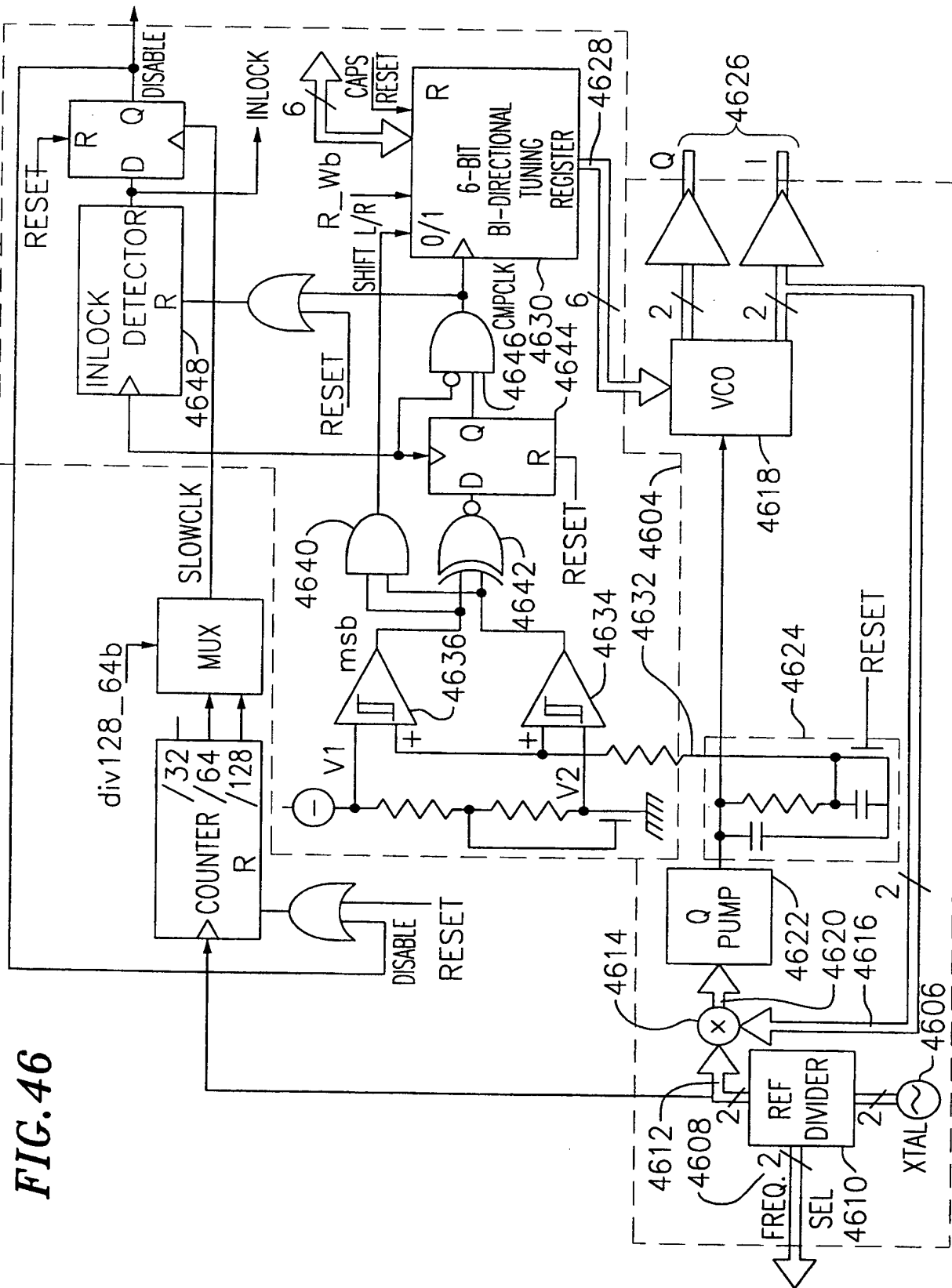




FIG. 47

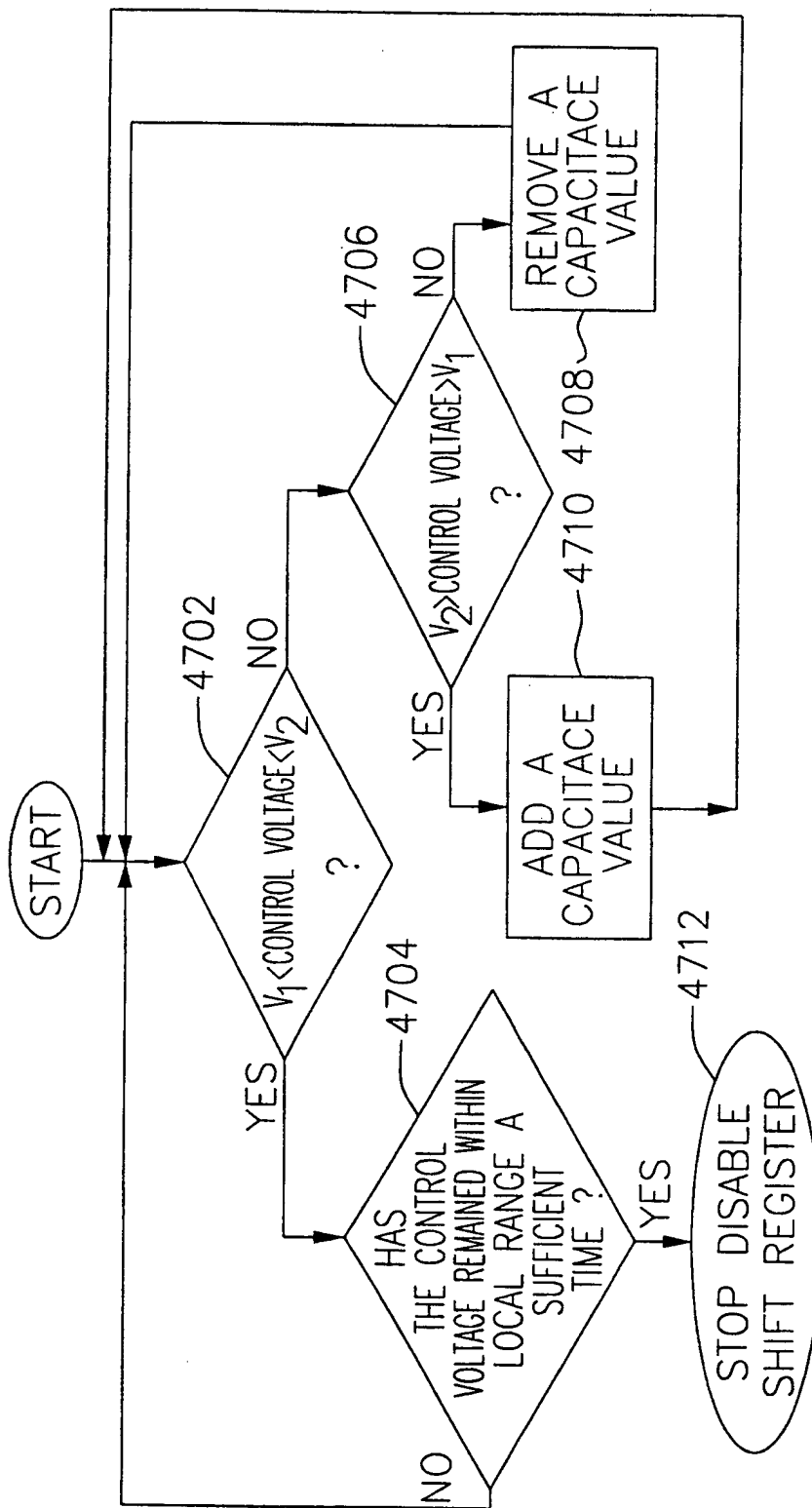




FIG. 48

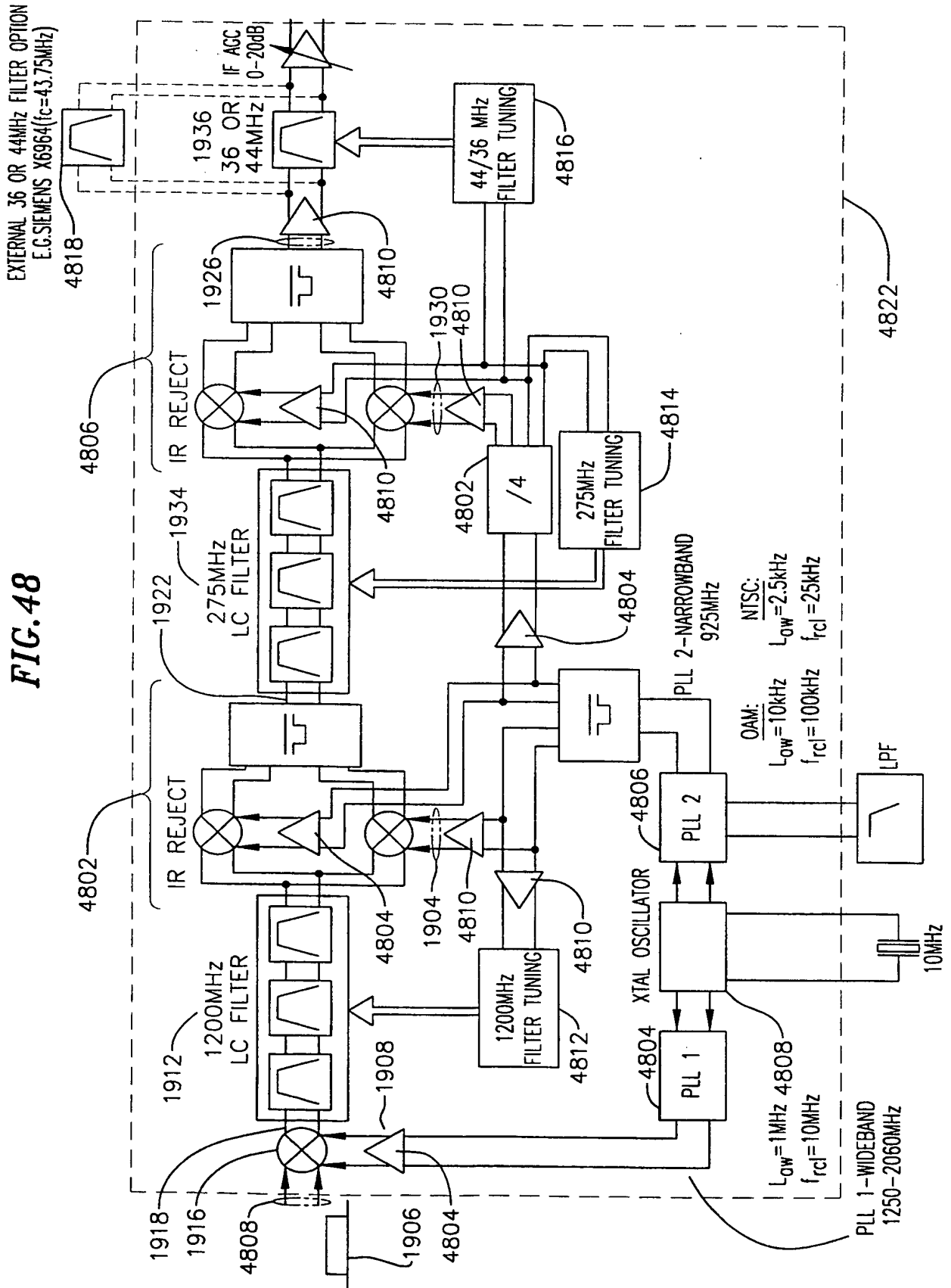


FIG. 49

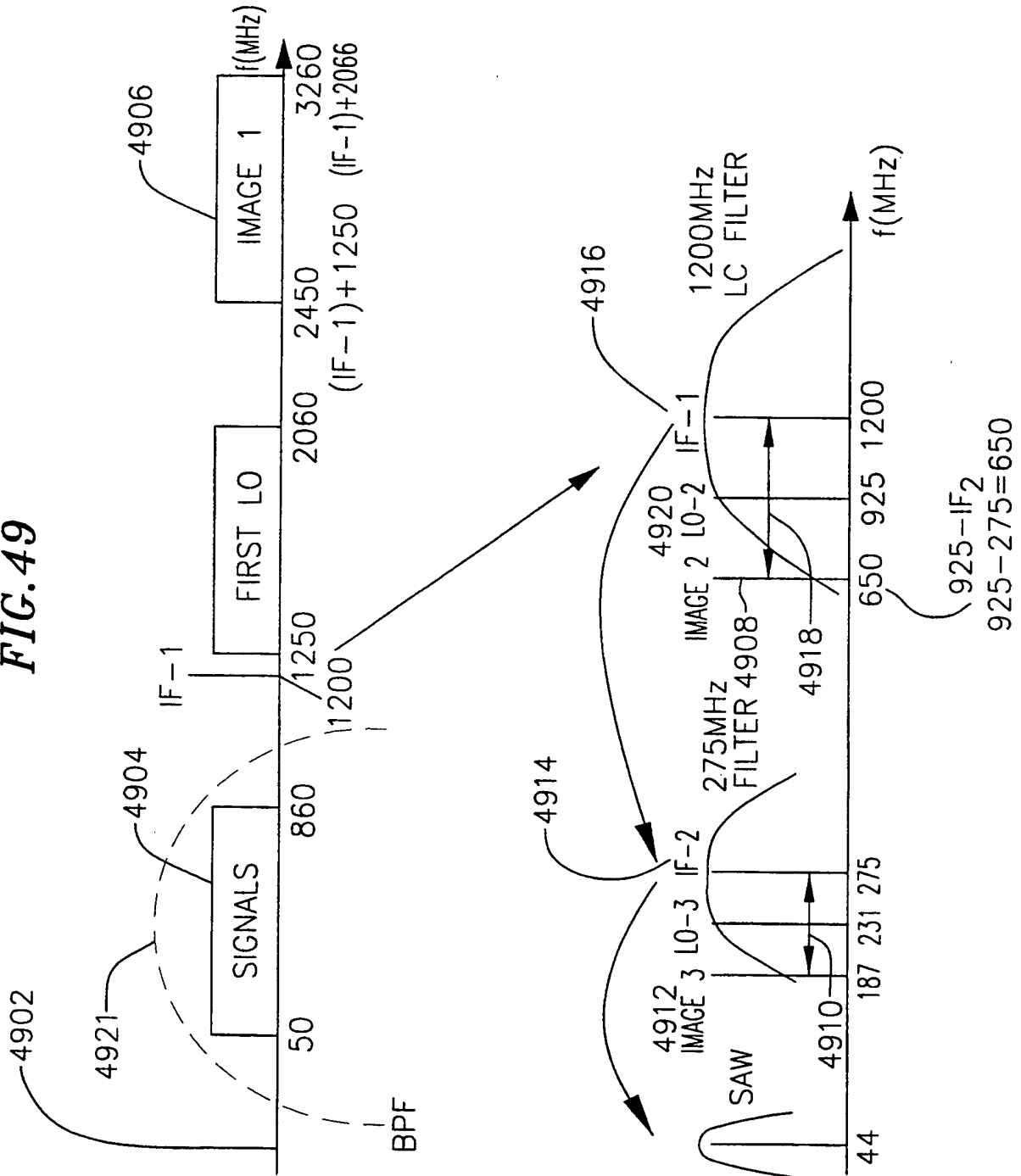
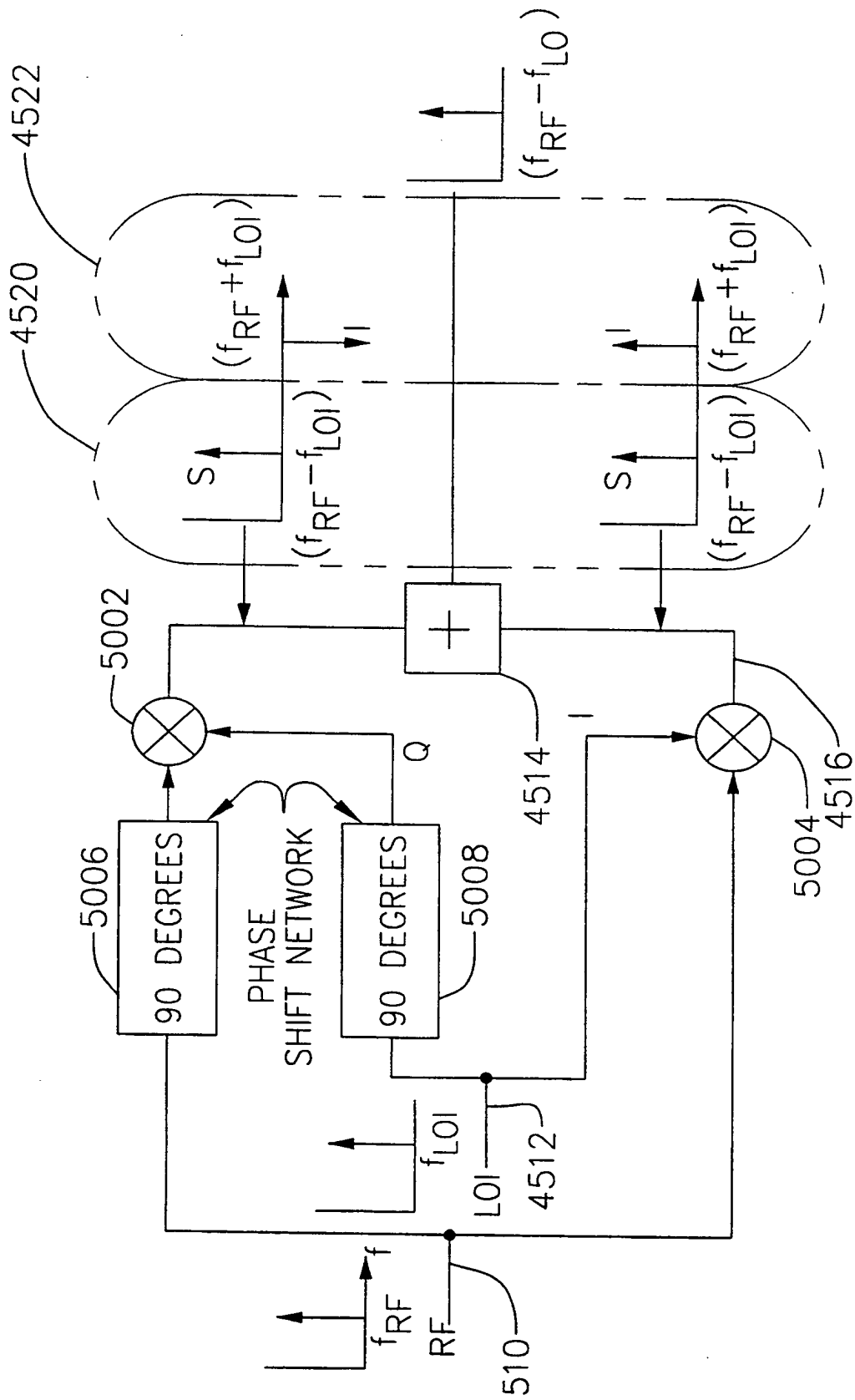
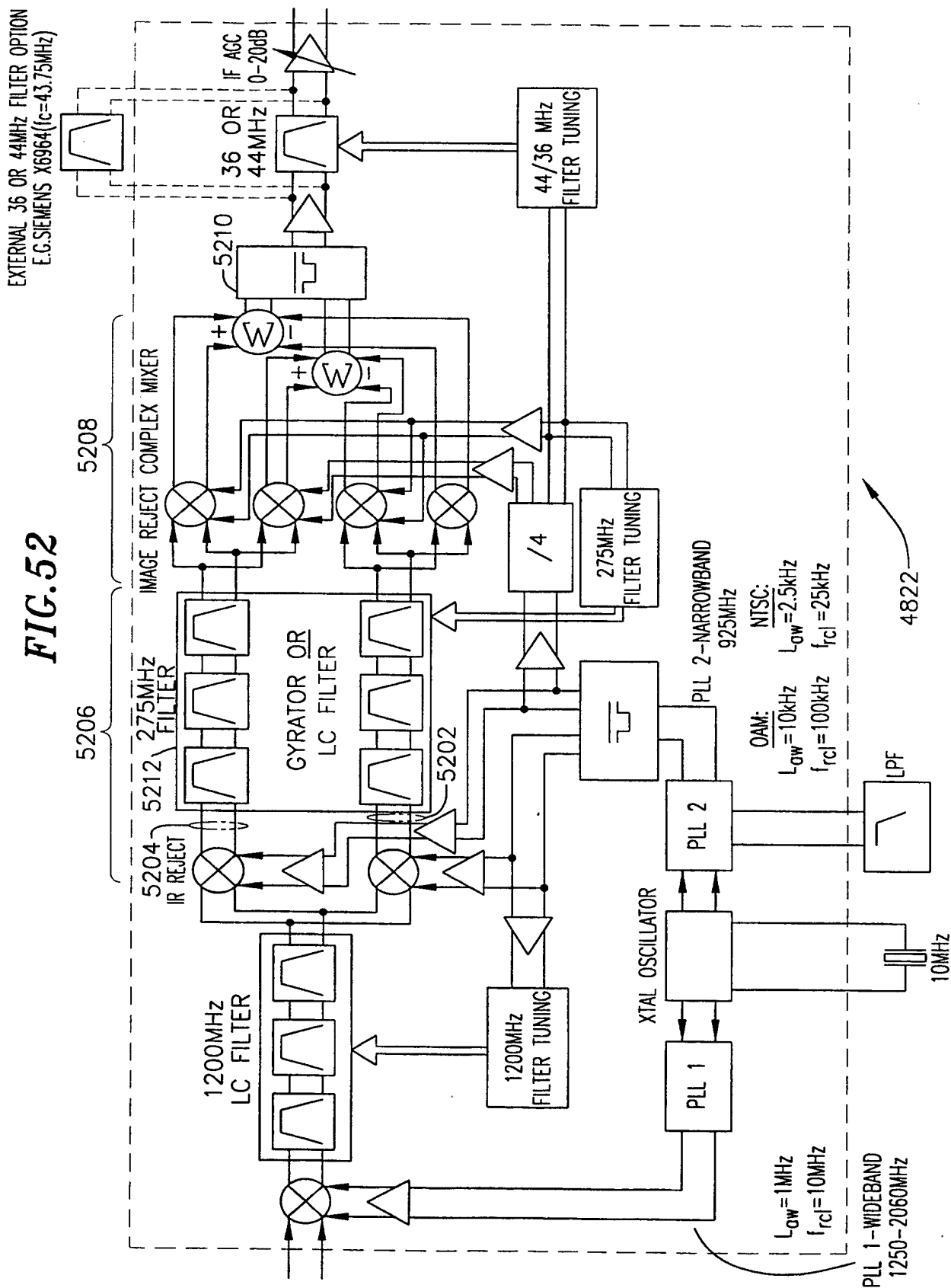




FIG. 50



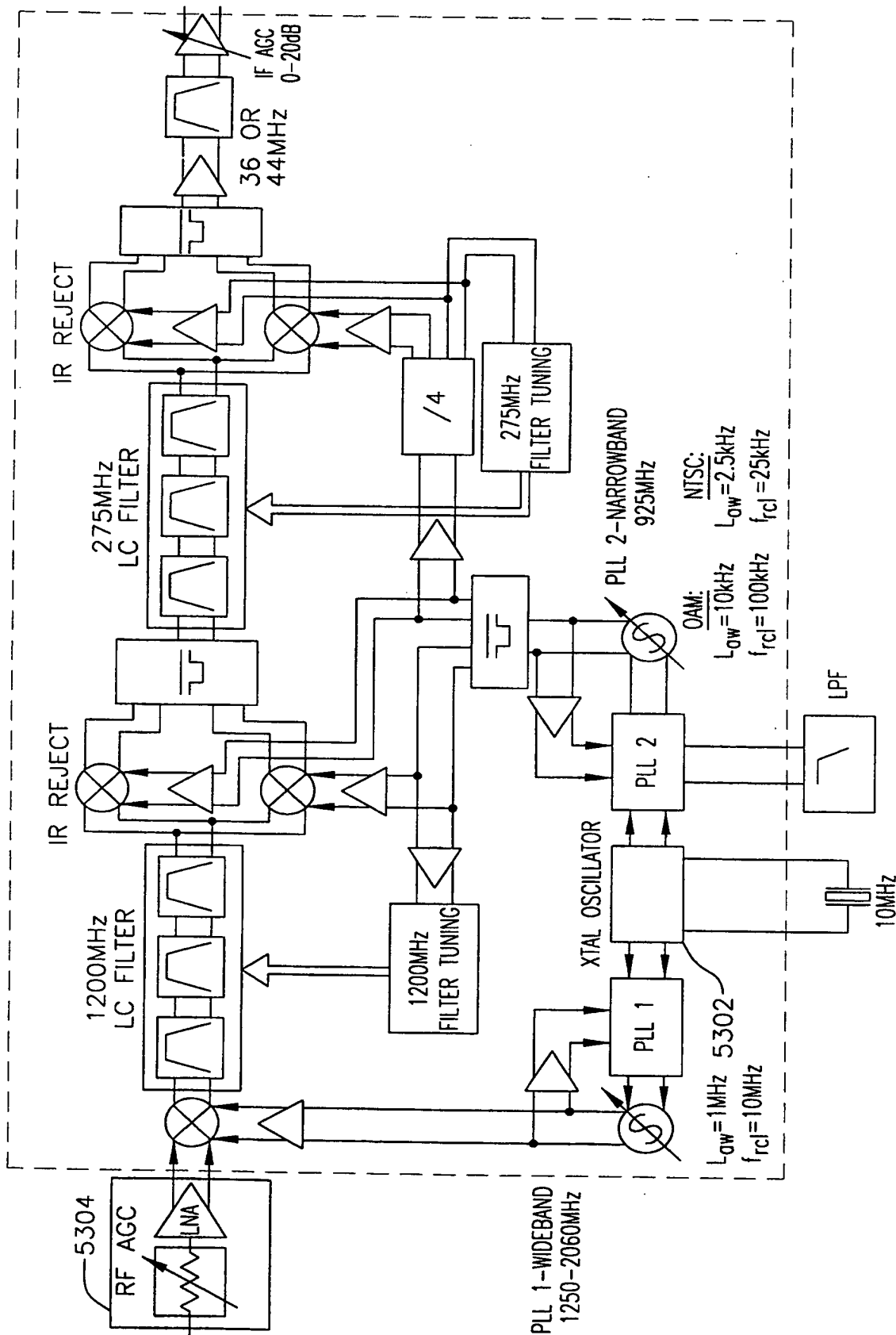




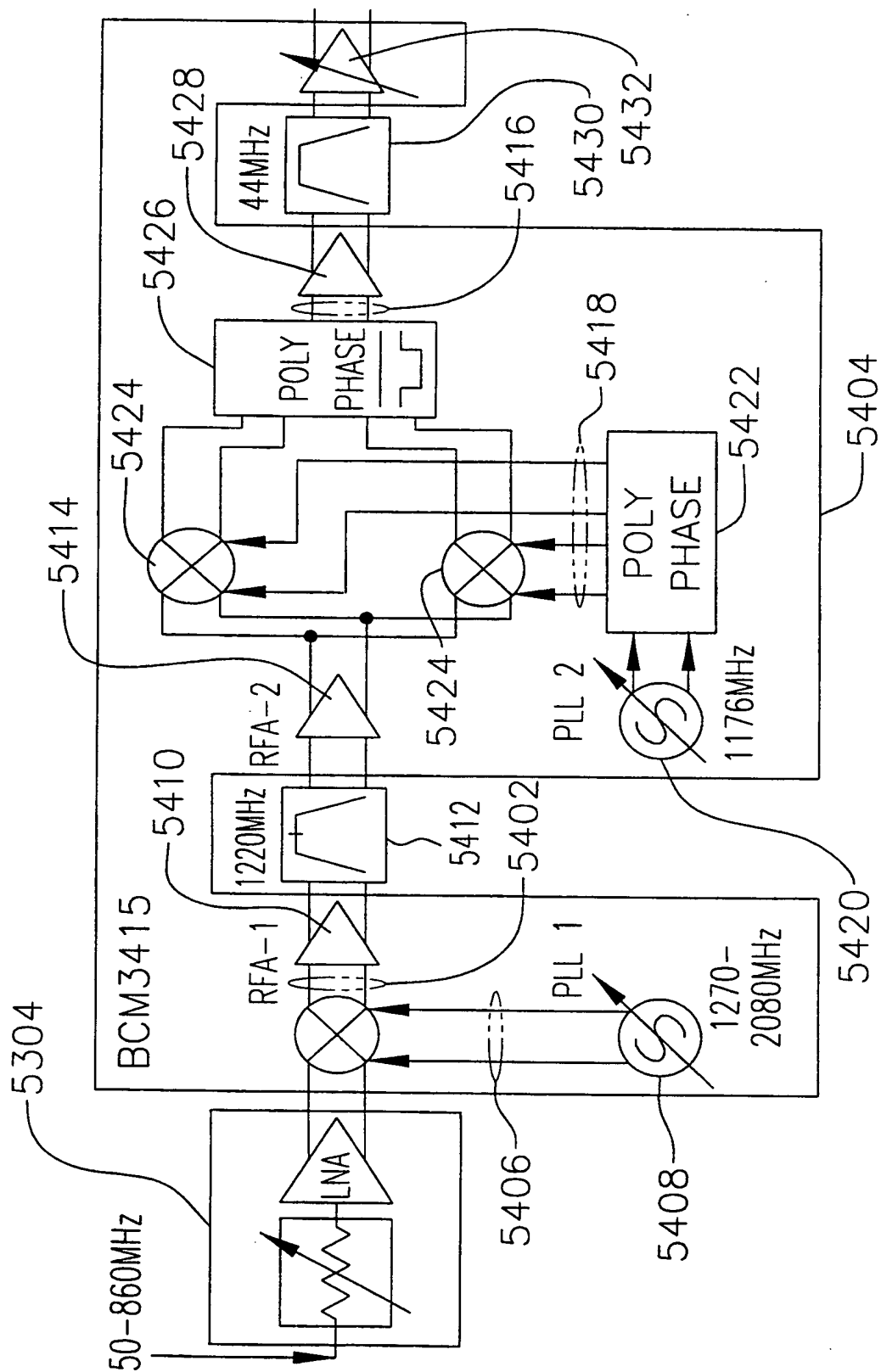


**FIG. 53**

CATV TUNER

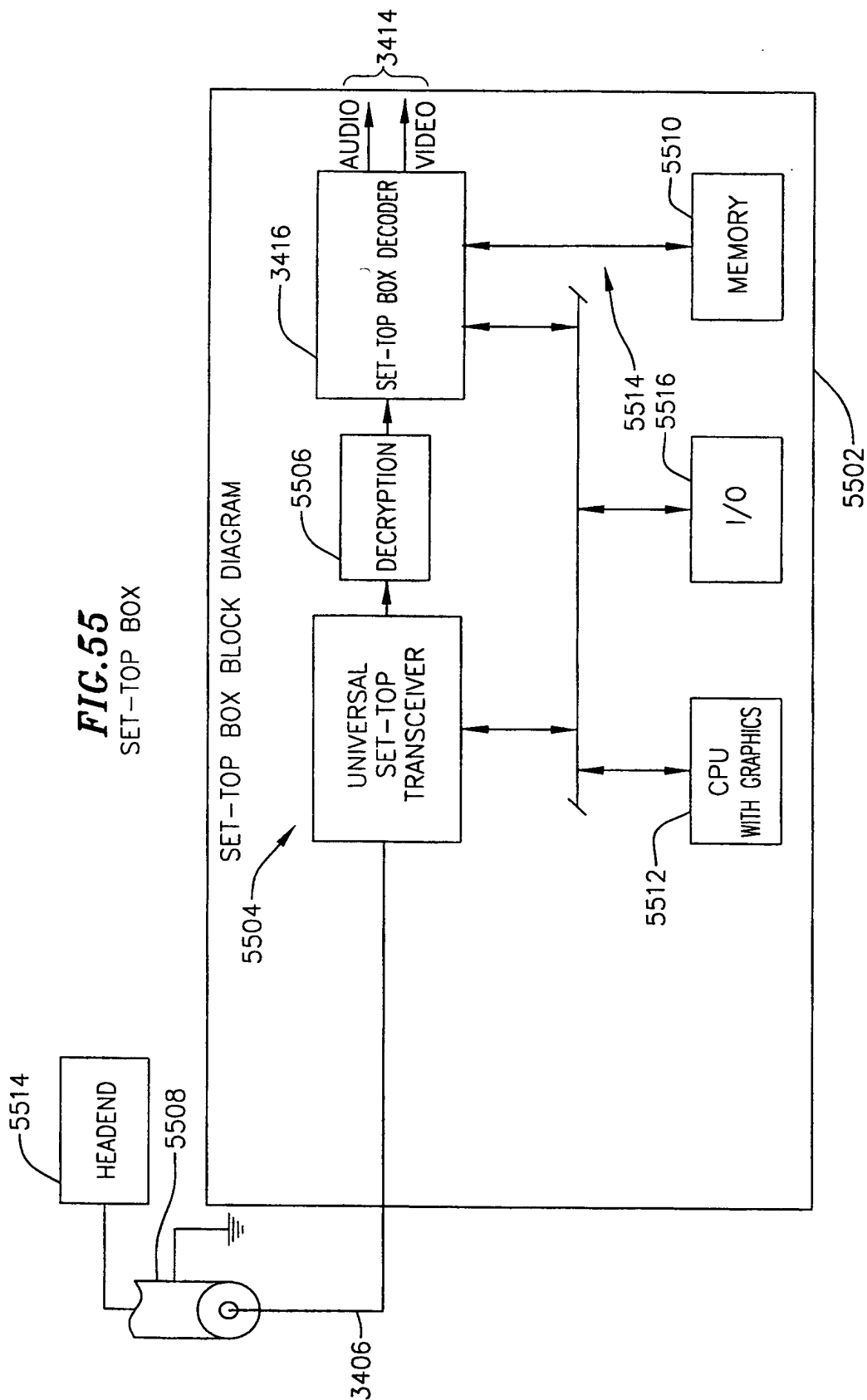


**FIG. 54**





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**FIG. 57**

VCR BLOCK DIAGRAM

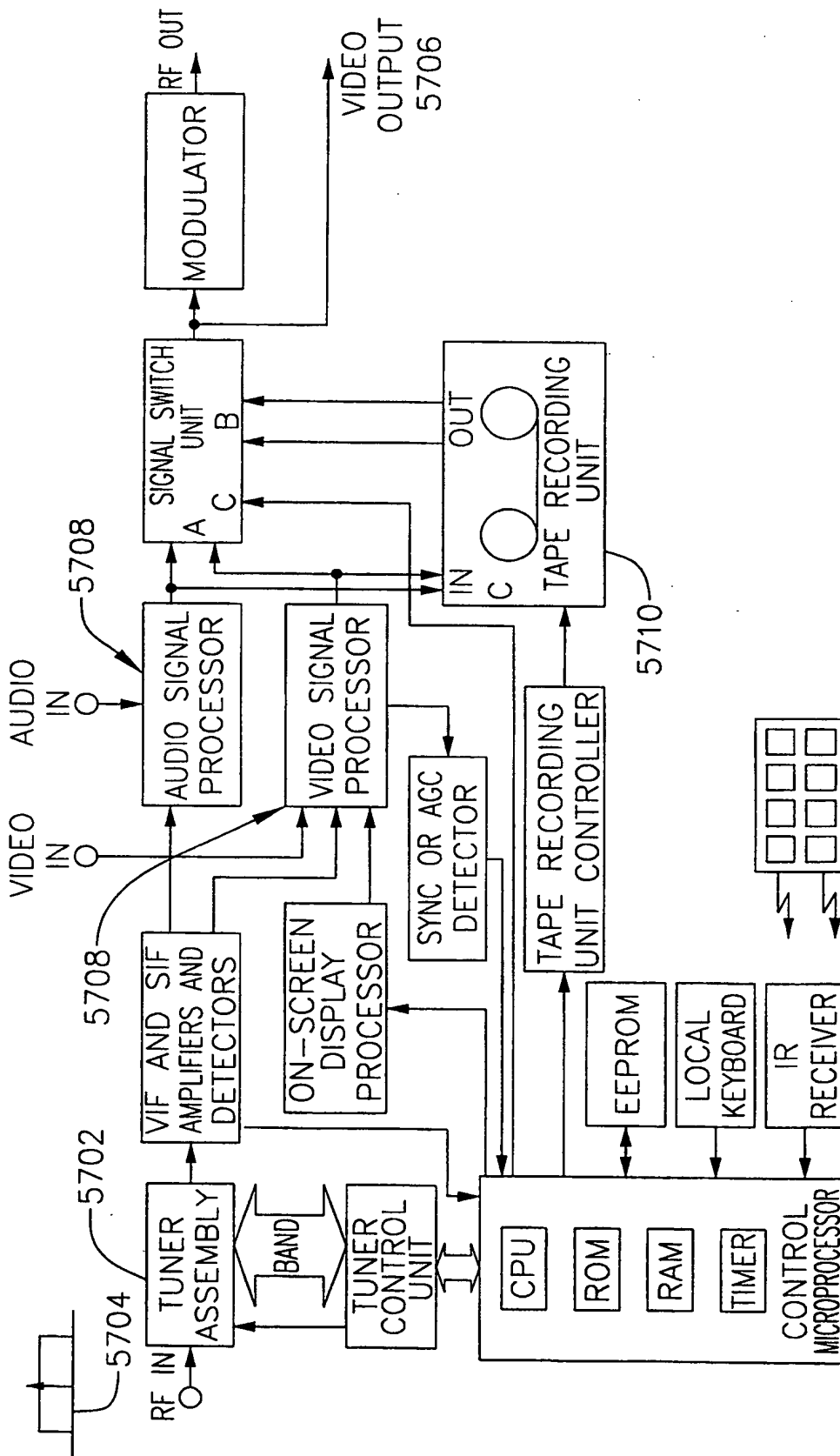
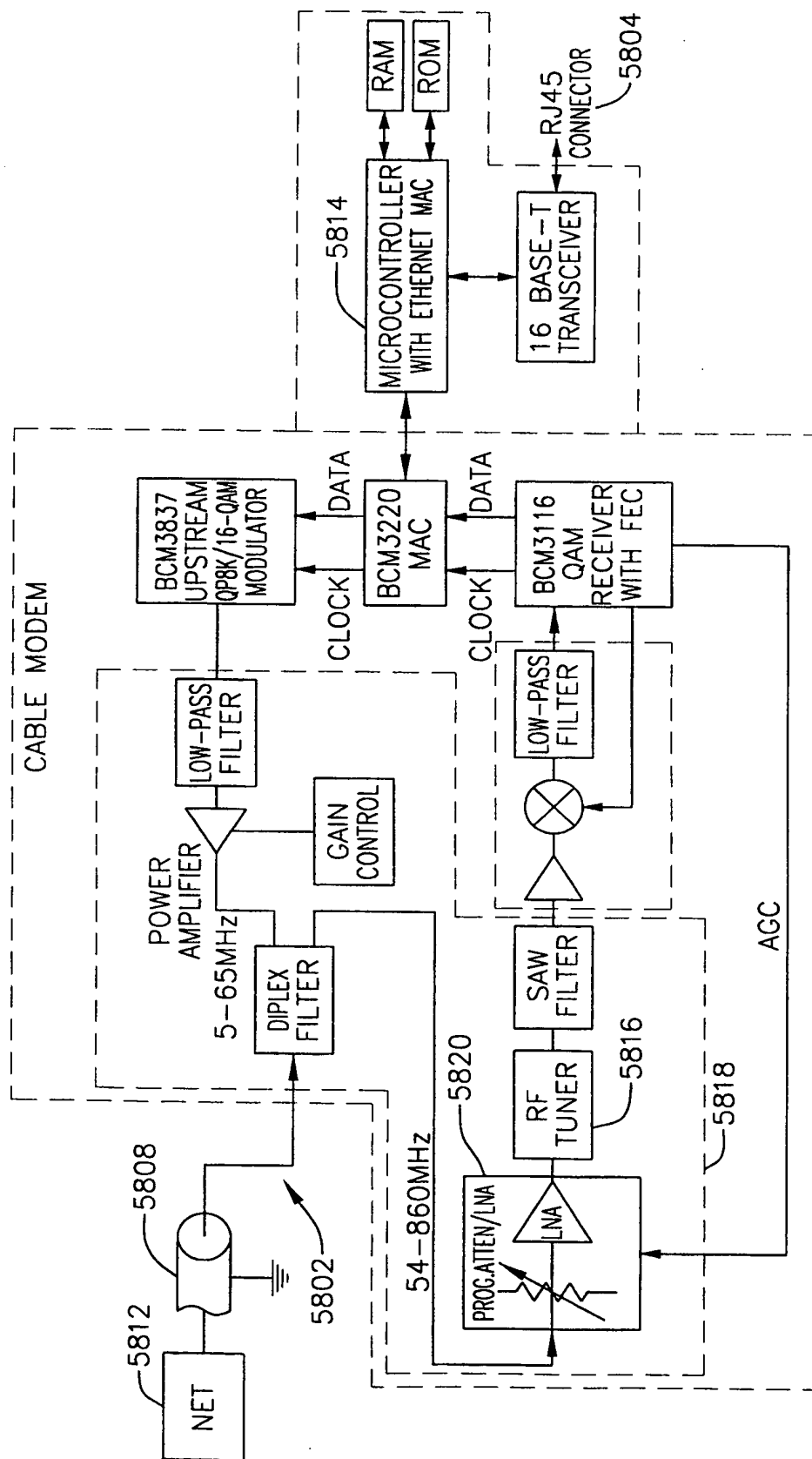


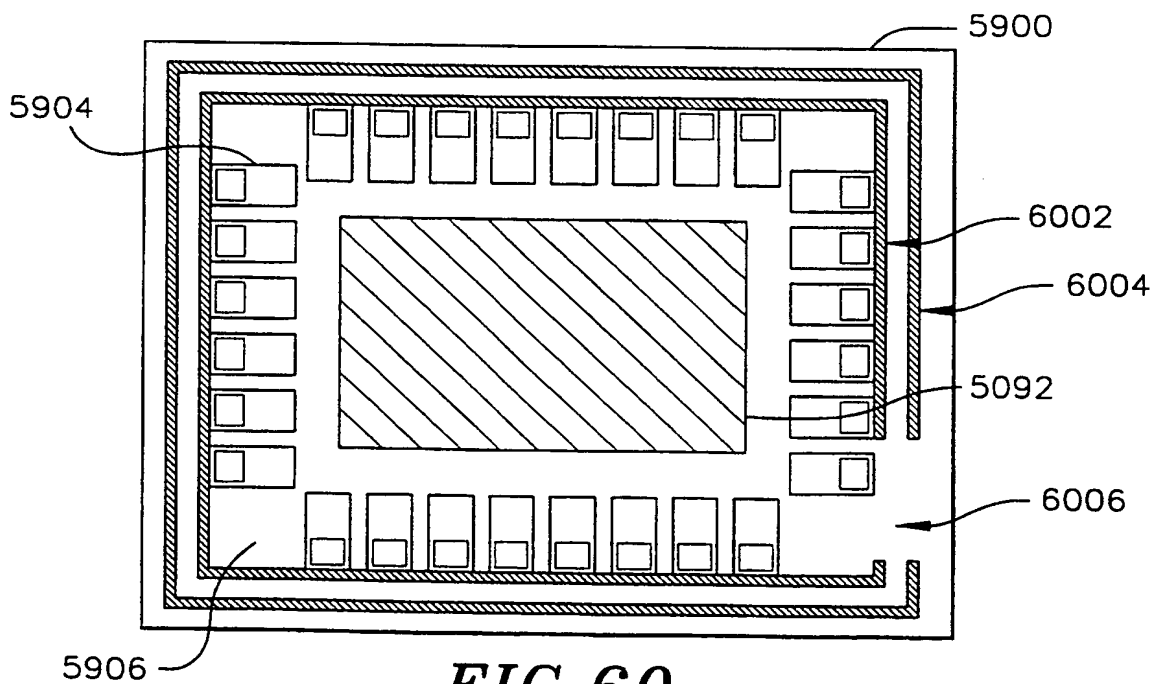
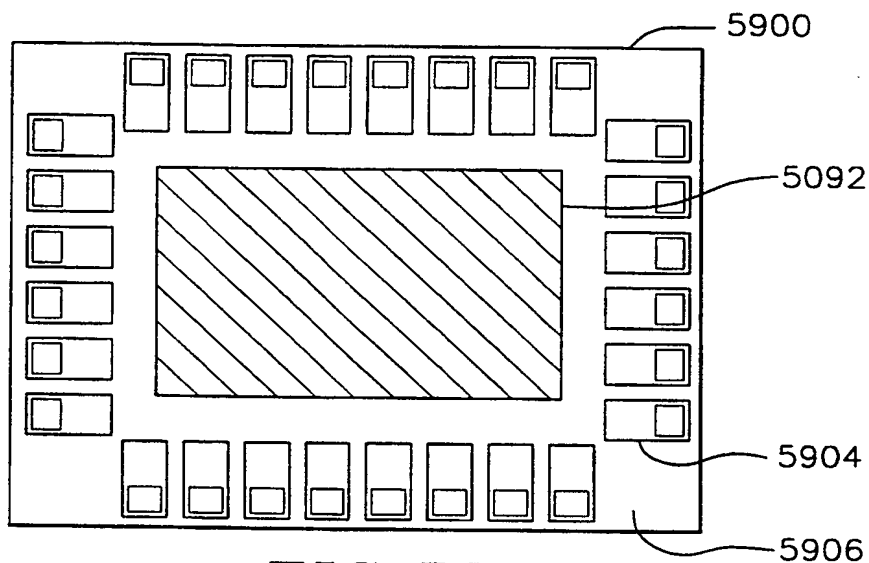


FIG. 58



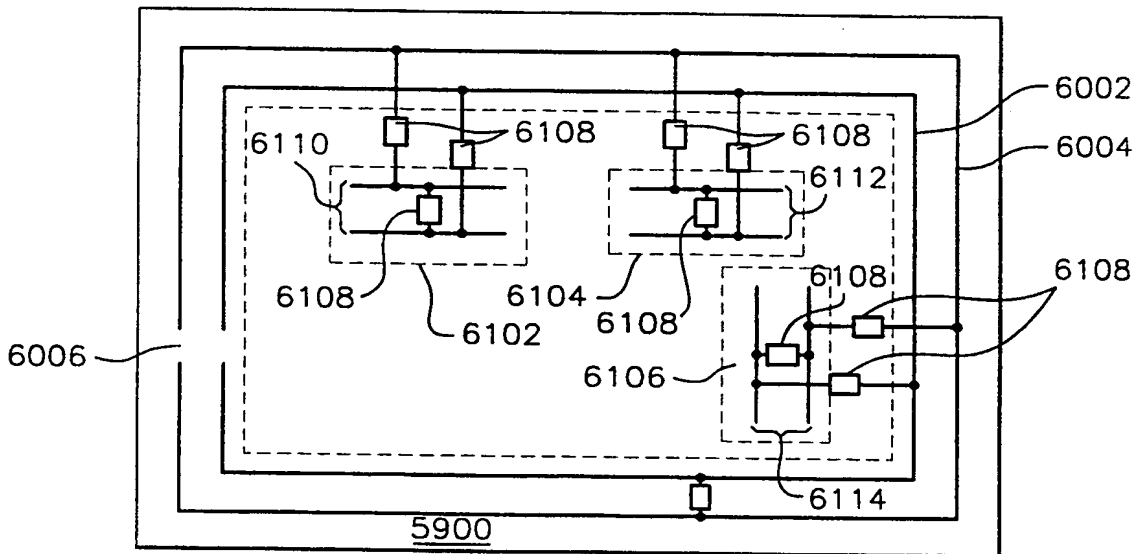


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**FIG. 61**



**FIG. 62**

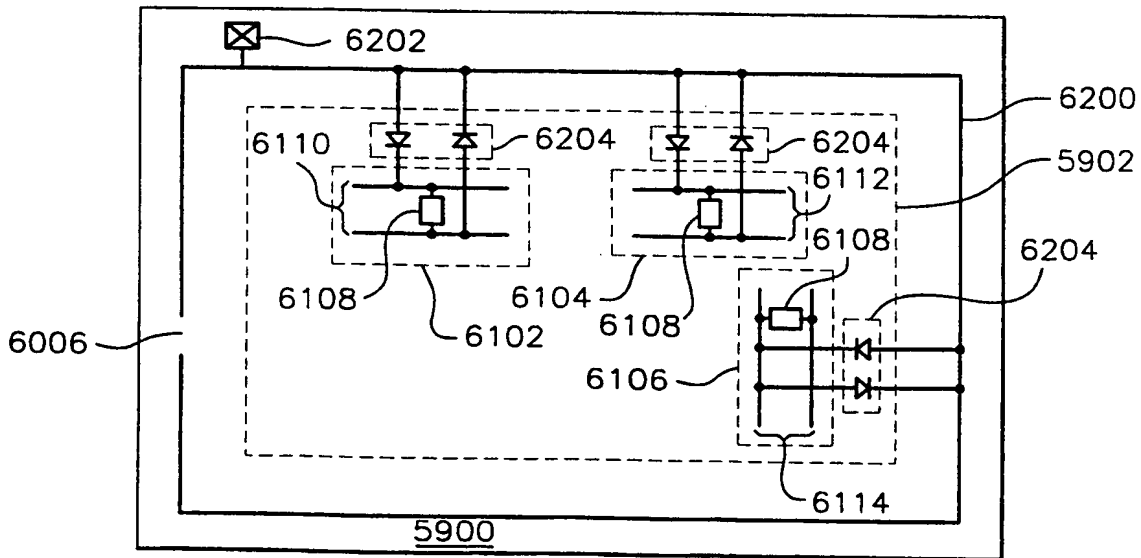
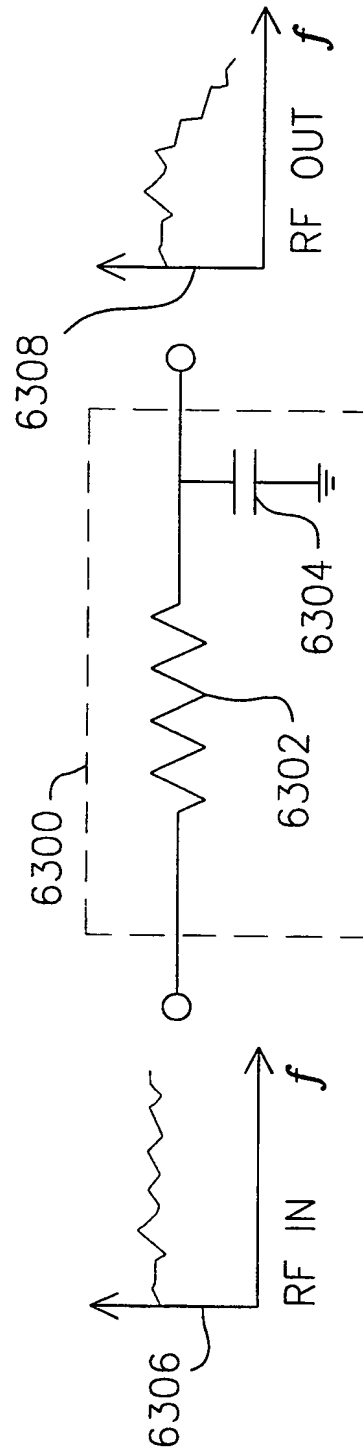


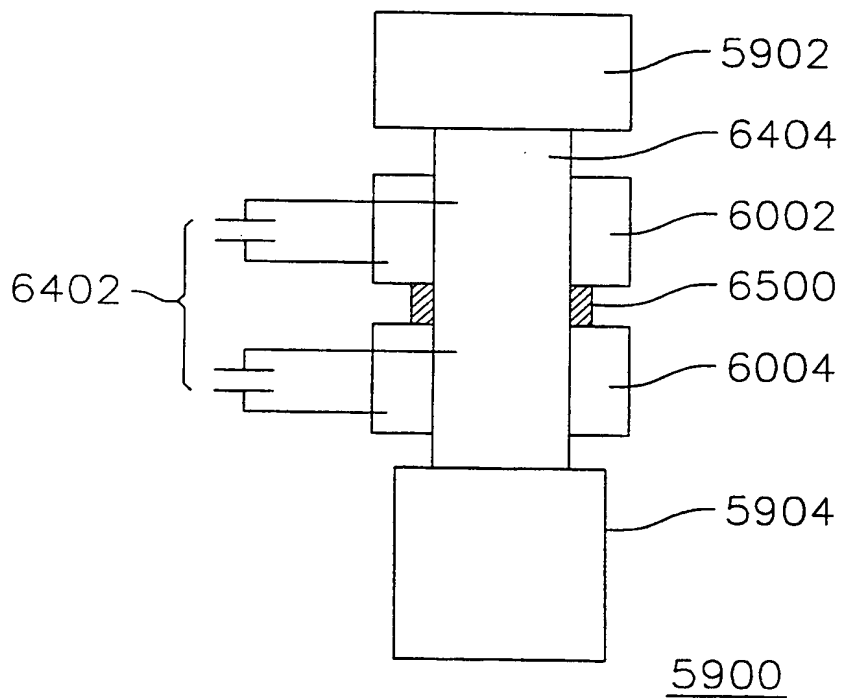


FIG. 63



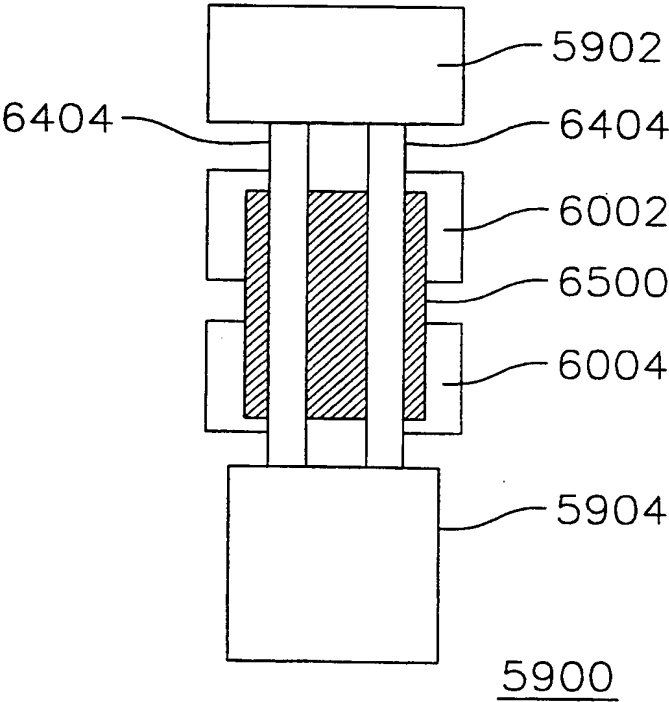


*FIG. 64*





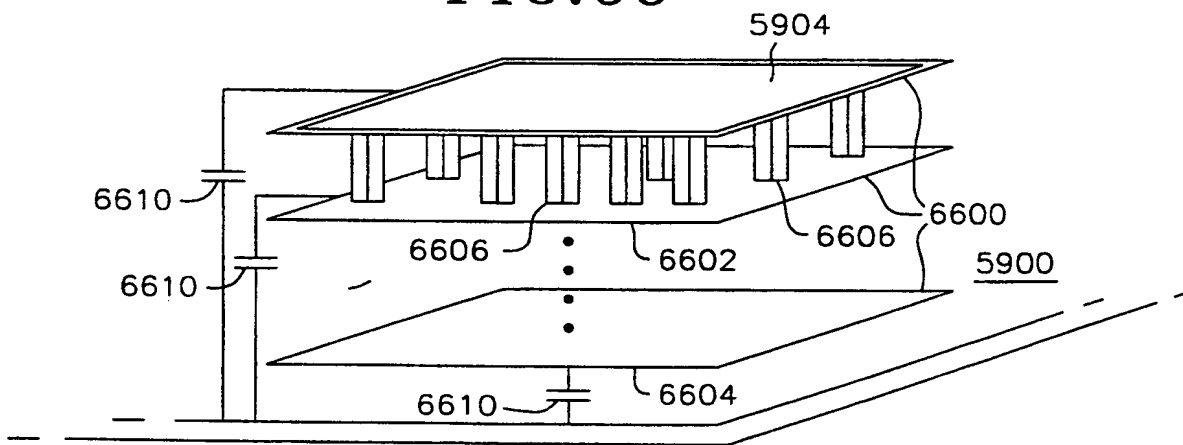
*FIG. 65*



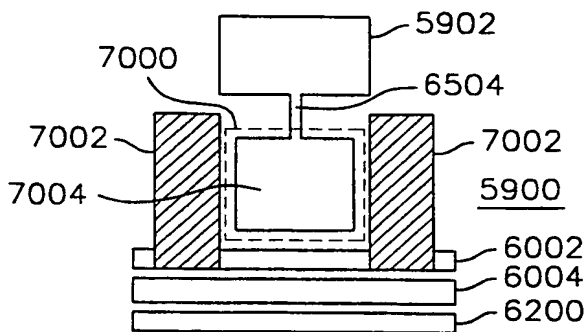


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**FIG. 66**

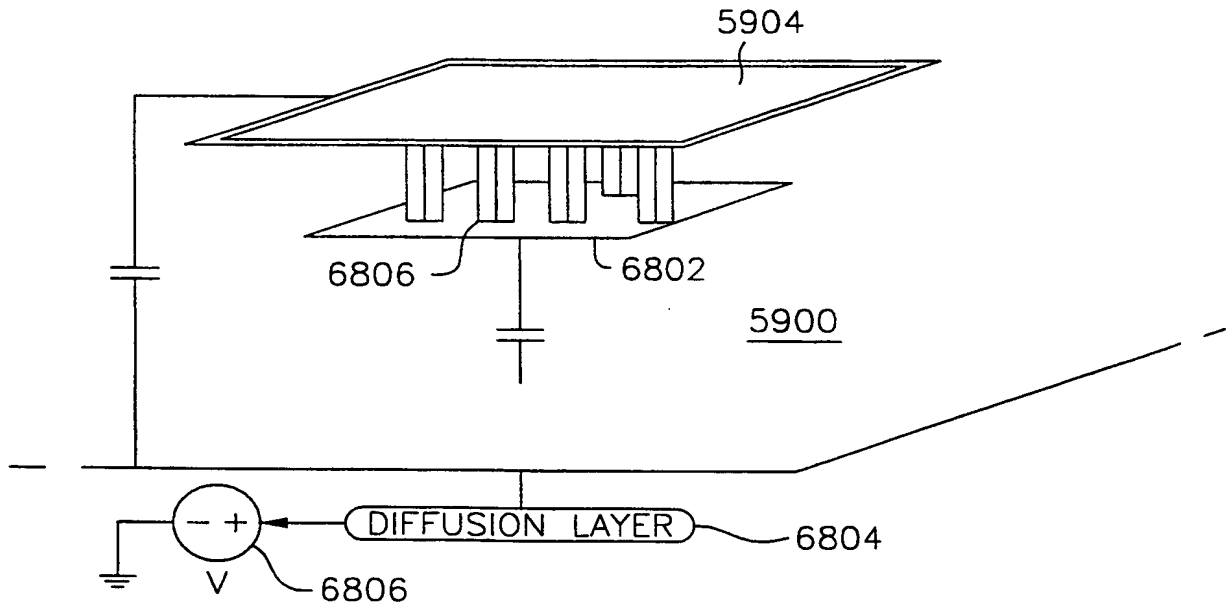


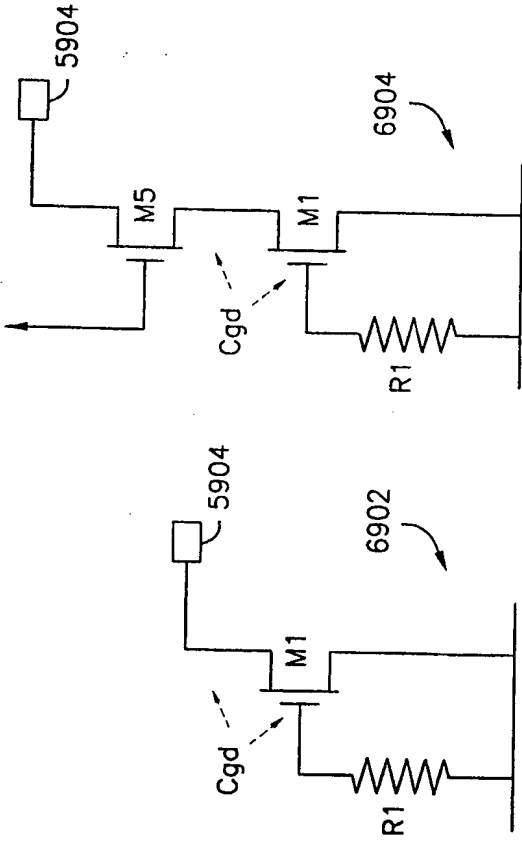
**FIG. 67**





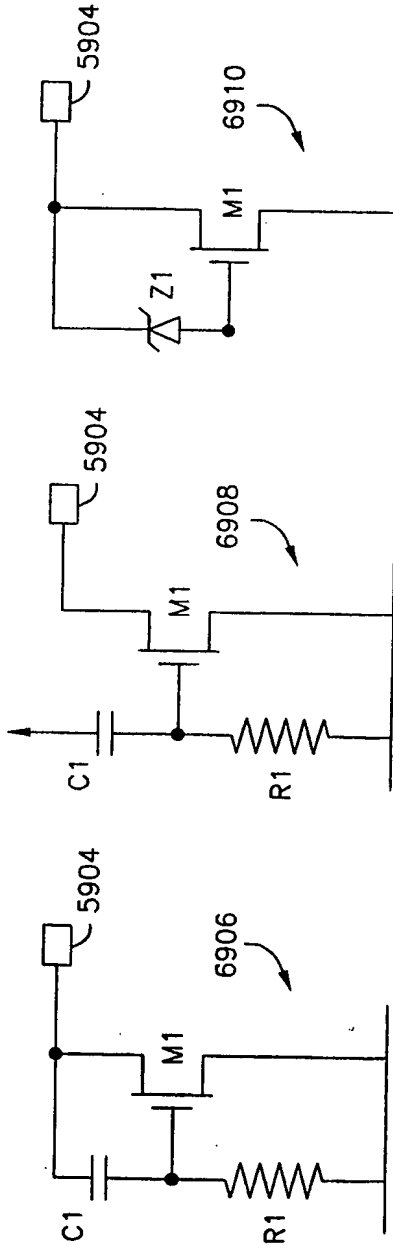
*FIG. 68*





**FIG. 69-2**  
PRIOR ART

**FIG. 69-1**  
PRIOR ART



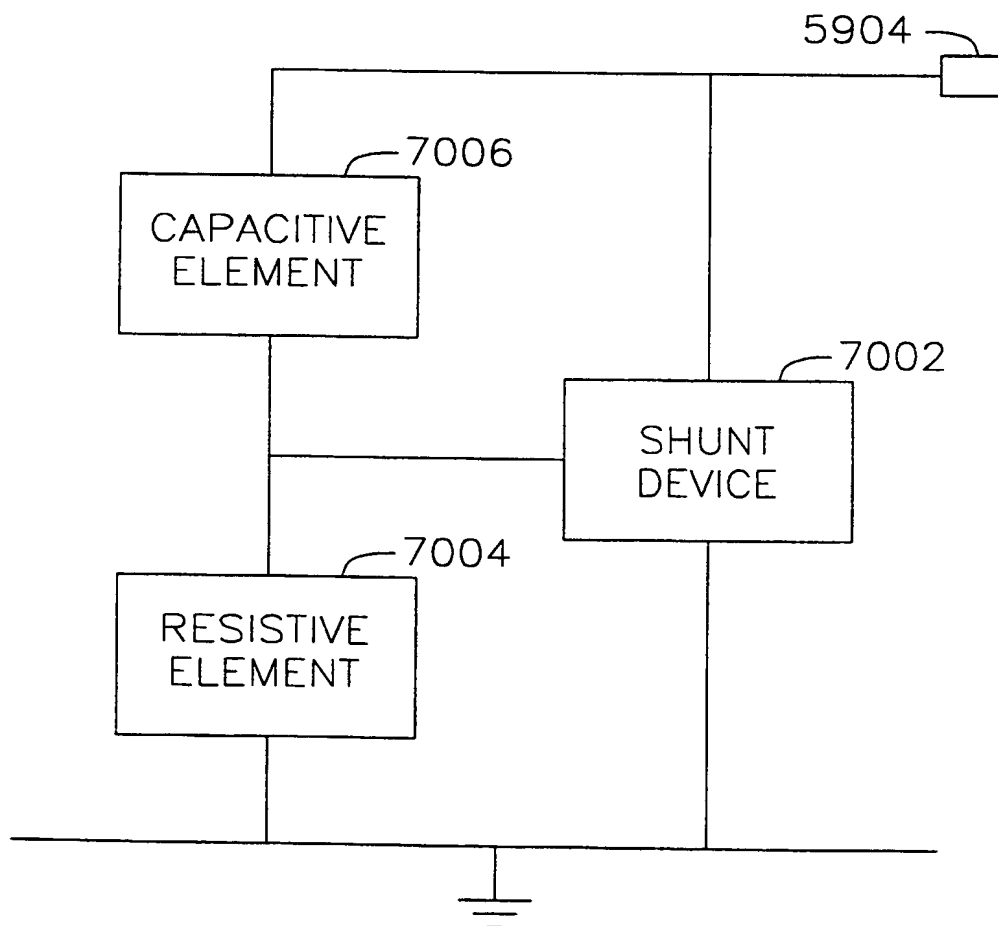
**FIG. 69-3**  
PRIOR ART

**FIG. 69-4**  
PRIOR ART

**FIG. 69-5**  
PRIOR ART

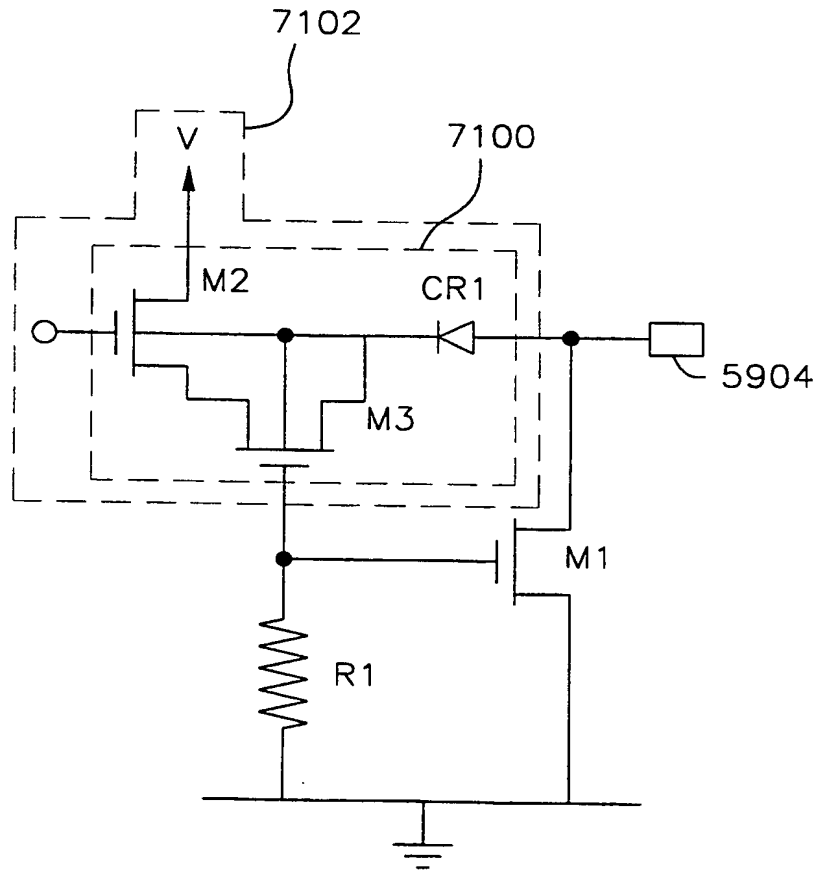


*FIG. 70*



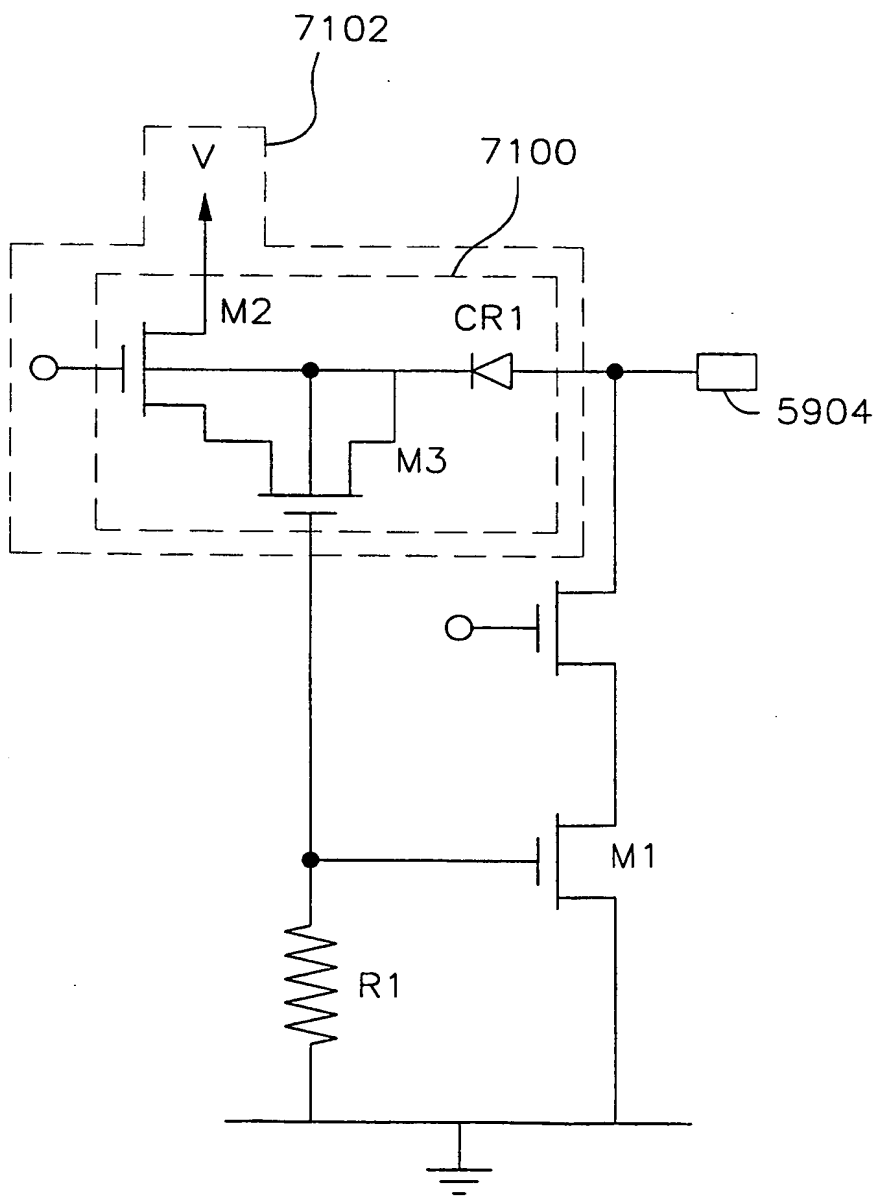


**FIG. 71**





*FIG. 72*





*FIG. 73*

